



PCB@

PCB 33A LA-J891P REV1 M/B 4
DAB00071010



LOGO@

ROYALTY HDMI W/LOGO+HDCP
RO0000003HM



X4E@

SMT EMC EG0 G1 G1R FOR EE AJ891 FH51M
X4EALYBOL01



X4EFP@

PCBA EMC EG0 G1 G1R W/FP AJ891 FH57M
X4EALYBOL51

Compal Confidential

MB Schematic Document

FH52M
LA-J891P

Rev:0.1

2019.09.25

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- VGA Port E
P. 39

HDMI - JHDMI1
- VGA Port C
HDMI
P. 40

VBIOS ROM
- SOP8
- Size : 1M
P. 29

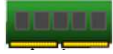
N18E-G0/G1/G1R
- MAX-Q
- GDDR6 6G/8G
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eDP - JEDP1
- CPU eDP
P. 38

**CoffeeLake H Processor
BGA1440 (42X28)
(CFL-H & CML-H_ 8+2)**
P. 6-13

Memory BUS

Interleaved (DDR4 2400/2666)


- DDR4 So-DIMM 260 pin
- Channel A
- BANK 0,1,2,3
- Address : 0XA0/1 P. 23


- DDR4 So-DIMM 260 pin
- Channel B
- BANK 4,5,6,7
- Address : 0XA3/4 P. 24

X4 DMI

**Cannonlake PCH - H
FCBGA874 (25X24)**
P. 14-21

**CFL-H : HM370
CML-H : HM470**

SPI ROM 16M
- SOP8
- Size : 16M
P. 16

SPI

LPC/eSPI BUS

TPM
- NPCT750
P. 66

EC KB9022
P. 58

I2C/PS2

Int.KBD
- KSI/KSO
- W/BL or 4 Zone RGB
P. 63

Extend IC
- I2C
- KC3810 P. 59

Fan Control*2
page 77

Touch Pad
- EC PS2
- PCH I2C1 P. 63

EMR - JEMR1
- PCH I2C0
P. 64

HD Audio

I2C

Type C - JTPEC1
- USB3.1 GEN2
- USB3.1 Port3&4
- RTS5441E
P. 42-43

USB3.1 - JUSB1
- GEN2
- On M/B
- Port 1
- W/USB Charger (SLGC55544)
P. 71

USB3.1 - JUSB2
- GEN2
- USB3.1 Port 5
- USB2.0 Port 3
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USB3.1 - JUSB3
- GEN2
- USB3.1 Port 2
- USB2.0 Port 2
P. 71

LAN(GbE) JRJ45
- PCIE 2.0 5GT/s
- Port 14
- E2600
P. 73

SSD - JSSD1 (PCIE)
- PCIE 2.0 5GT/s
- PCIE Port 21-24
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SSD - JSSD2 (PCIE/SATA)
- PCIE 2.0 5GT/s
- PCIE Port 9-12
- SATA @ Port 12
P. 68

SSD - JSSD3 (PCIE/SATA)
- PCIE 2.0 5GT/s
- PCIE Port 17-20
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HDD - JHDD1
- SATA 3.0
- Port 13 (SATA 0B)
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HDA Codec
- ALC295
P. 56

Audio Jack
- On IO/B

Int. DMIC
- On CCD Module

Int. Speaker
- ON IO/B > L
- ON M/B > R

Tuch Screen
- USB2 Port 6
- PCH I2C2
P. 38

Finger print
- USB2 Port 8
P. 66

DDC Camera
- Port 5
P. 38

WIFI - JNGFF1
- PCIE1.0 2.5GT/s
- PCIE Port 15
P. 52

Sub Board	
IO/B (JIO1/JIO2)	P. 73
HS/B (JHS1)	P. 66
TURBO/B (JTURBO1)	P. 77
RTC CKT. (JRTC1)	
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Power On/Of f CKT	
	P. 63
HW Circuit DC/DC	
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Power Circuit DC/DC	
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Vcc Ra	3.3V +/- 5%	EC Board ID Table for AD channel				
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD	
0	0	0.000 V	0.300 V	0x00 - 0x13		
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76	
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87	
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96	
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4	
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF	
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7	
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9	
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4	
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD	
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFF	
19	NC	3.000 V	3.000 V	0xFF1 - 0xFF		

Board ID	PCB Revision
0	50 Rev0.1
1	50 Rev0.2
2	50 Rev0.3
3	50 Rev1.0
4	50 Rev0.2+RGB
5	50 Rev0.3+RGB
6	50 Rev1.0+RGB
7	60 Rev0.1
8	60 Rev0.2
9	60 Rev0.3
10	60 Rev1.0
11	60 Rev0.2+RGB
12	60 Rev0.3+RGB
13	60 Rev1.0+RGB
14	
15	
16	
17	
18	
19	
*PCB Version *Key board type	

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.					

BUS	Device	Address(7 bit)	Address(8bit)	
I2C_0 (+3VS)			Write	Read
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
PCH_SMBCLK (+3VS)	SA577C-12A0 (Touch Pad)			
	DIMM1			
	DIMM2			
PCH_SML1CLK	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
EC_SMB_CK2 (+3VS)	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	LED driver	0xC0		

KC3810 0xC0

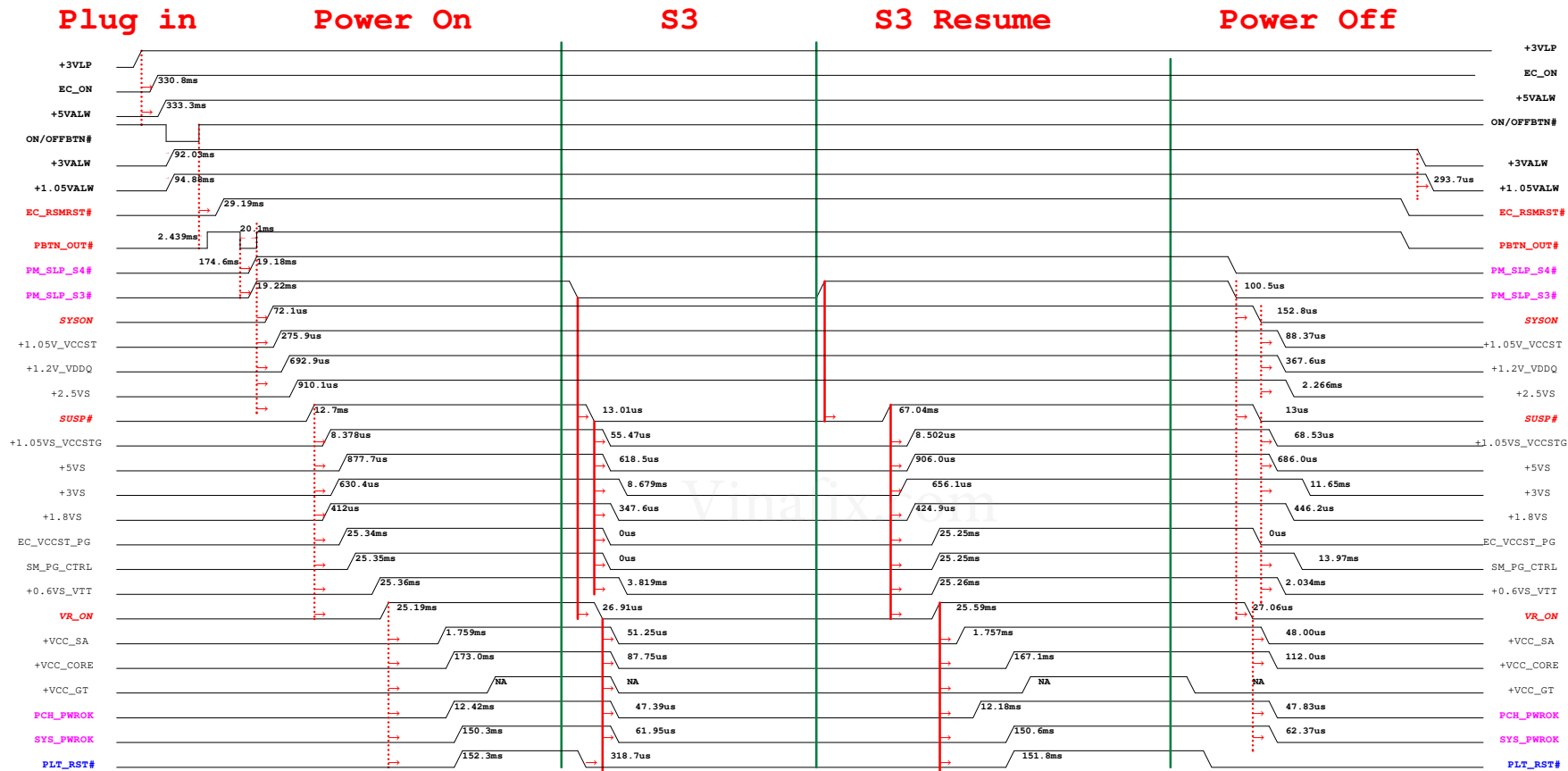
Item (X43)	BOM Structure	Item (X43)	BOM Structure
Unpop	@	eDP-TS USB	TS_USB@
Connector	CONN@	eDP-TS USB	NONTS_I2C@ V
PCB	PCB@ V	eDP-TS I2C	TS_I2C@
UMA Only(Reserved)	UMA@	mDP	DP@
H62 CPU(Reserved)	H62@	For Acer IOAC	IOAC@ V
H82 CPU(POP)	H82@ V	No Acer IOAC	NIOAC@
Board ID	DVT@	Intel CNVi	CNVi@ V
Board ID RGB	DVTRGB@	FOR UART BT module	UART_BT@
		FOR UART debug	UART@
CFL i5QS CPU QRR5	i5QS@	Extend GPIO	KC3810@
CFL QS PCH	PCHQS@		
CML i5 CPU QJT1	CMLi5@	Finger Print	FP@
CML i7 CPU QJT2	CMLi7@	FingerPrint(with PBA)	PBA@ V
CML i9 CPU QJT0	CMLi9@	KB backlight	KBLED@ V
CML PCH	CMLPCH@	KB LED driver	LED14P@
dGPU circuit	VGA@ V	EMR 1.8V	WC18V@
GPU_N18E-G0	N18EG0@/G0@	EMR 3.3V	WC33V@
GPU_N18E-G1B	N18EG1B@/G1B@	Thermal sensor	TMS@ V
GPU_N18E-G1R	N18EG1R@/G0@/G1B@	TPM pop	TPM@
		TPM non-pop	NTPM@ V
		SSD3 pop	SSD3@
GC6(POP)	FGC6@ V		
GC6(Reserved)	NFGC6@		
		435P4RBOL01(IO/B)	
		X4EP4RBOL01(IO/B)	

43 Level	Descript i on
431ALYBOL03	SMT MB AJ891 FH51M EG0MP 6G QTJ2 HDMI
431ALYBOL08	SMT MB AJ891 FH51M EG0 6G QTJ1 HDMI
431ALYBOL09	SMT MB AJ891 FH51M EG1B 6G QTJ2 RGB HDMI
431ALYBOL51	SMT MB AJ891 FH53M EG0MP 6G QTJ1 HDMI
431ALYBOL52	SMT MB AJ891 FH53M EG1B MP 6G QTJ2 HDMI
431ALYBOL53	SMT MB AJ891 FH53M EG1R PS 8G QTJ2 HDMI
431ALYBOLA1	SMT MB AJ891 FH52M N18EG0 6G QTJ1 HDMI
431ALYBOLA2	SMT MB AJ891 FH52M N18EG0 6G QTJ2 HDMI
431ALYBOLA3	SMT MB AJ891 FH52M N18EG1B 6G QTJ2 HDMI
431ALYBOLC1	SMT MB AJ891 FH57M i5 EGO 6G HDMI
431ALYBOLC2	SMT MB AJ891 FH57M i7 G1B 6G HDMI
431ALYBOLC3	SMT MB AJ891 FH57M i7 G1R 8G W/FP HDMI
431ALYBOLC4	SMT MB AJ891 FH57M i7 G1R 8G W/FP HDMI

Item (X4E)	BOM Structure
EMI requirement	EMI@ V
EMI require reserve	XEMI@
ESD requirement	ESD@ V
ESD require reserve	XESD@
FP ESD requirement	FPESD@ V
X4EALYBOL01(wo/FP)	X4E@ V
X4EALYBOL51(w/FP)	X4EFP@ V

Item (X76)	BOM Structure
VRAM-MICRON(1.2V)	MIC_G1B@;MIC_G1R@/X76_MIC@
VRAM-SAMSUNG(1.2V)	SAM_G1B@;SAM_G1R@/X76_SAM@
VRAM-MICRON(1.35V)	MIC_G0@/X76_MIC@
VRAM-SAMSUNG(1.35V)	SAM_G0@/X76_SAM@
OVRM-ON	ON@
OVRM-uPI	uPI@

X76869BOL05 - MICRON 6G 1.2V	X76L05@	
X76869BOL06 - SAMSUNG 6G 1.2V	X76L06@	G1B
X76869BOL07 - MICRON 8G 1.2V	X76L07@	
X76869BOL08 - SAMSUNG 8G 1.2V	X76L08@	G1R
X76869BOL11 - MICRON 6G 1.35V	X76L11@	
X76869BOL12 - SAMSUNG 6G 1.35V	X76L12@	G0
X76869BOL09 - ON OVRM	X76L09@	
X76869BOL10 - uPI OVRM	X76L10@	OVRM

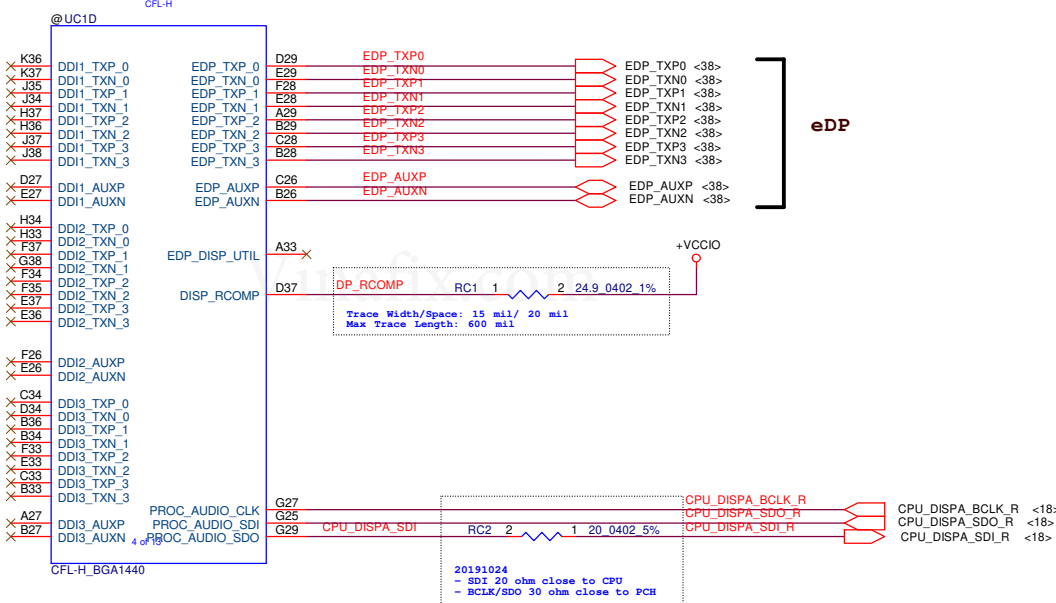


Coffee Lake-H
- Re-fresh R0 stepping

UC1
S QS@
S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00
UH1
S PCHQS@
S IC FHMM370 QNYF B0 BGA 874P PCH-
SA0000BPF10

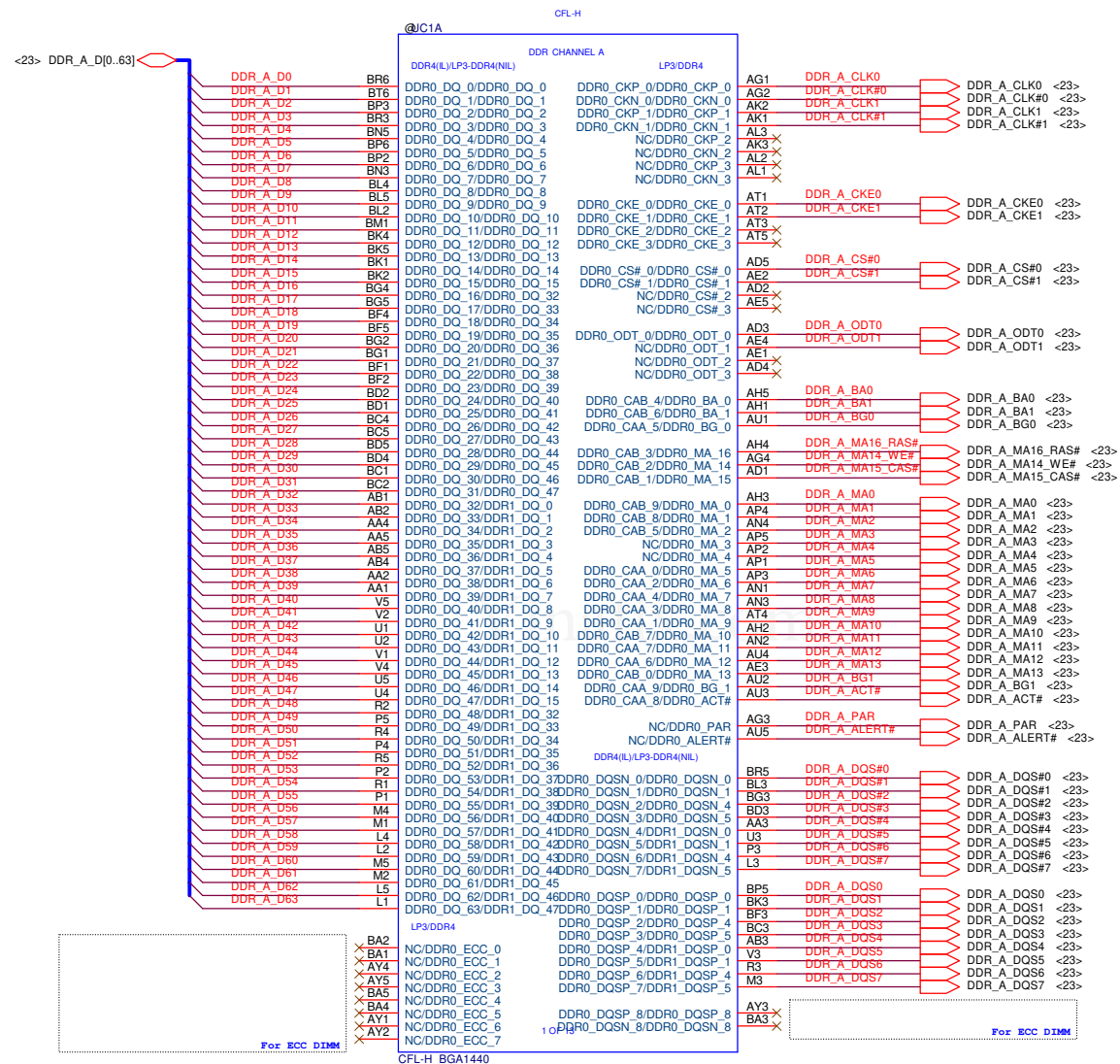
Comet Lake-H

UC1
S CMLI5@
S IC CL8070104398806 QTJ1 R0 2.1G 1440 S
SA0000D3H10
UC1
S CMLI7@
S IC CL8070104398908 QTJ2 R0 2.4G 1440 S
SA0000D3N10
UC1
S CMLI9@
S IC CL8070104399007 QTJ0 R0 2.8G S
SA0000D3G10
UH1
S CMLPCH@
S IC FHSSKU_MBL QS64 A0 FCBGA 874P S
SA0000D3F10



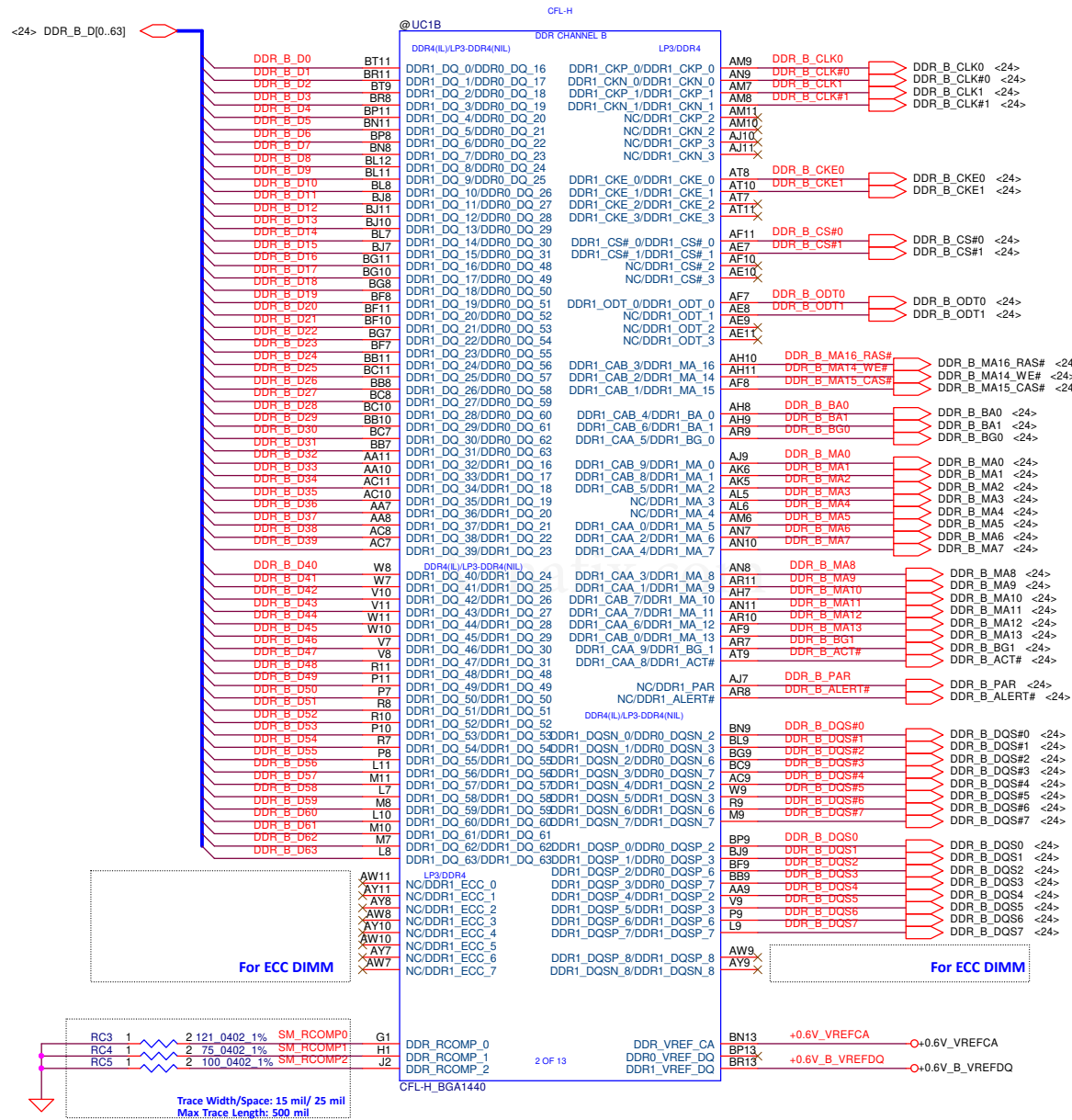
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CHANNEL-A Interleaved Memory



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				FH51M M/B LA-J871P		0.1
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CHANNEL-B Interleaved Memory

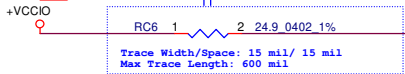
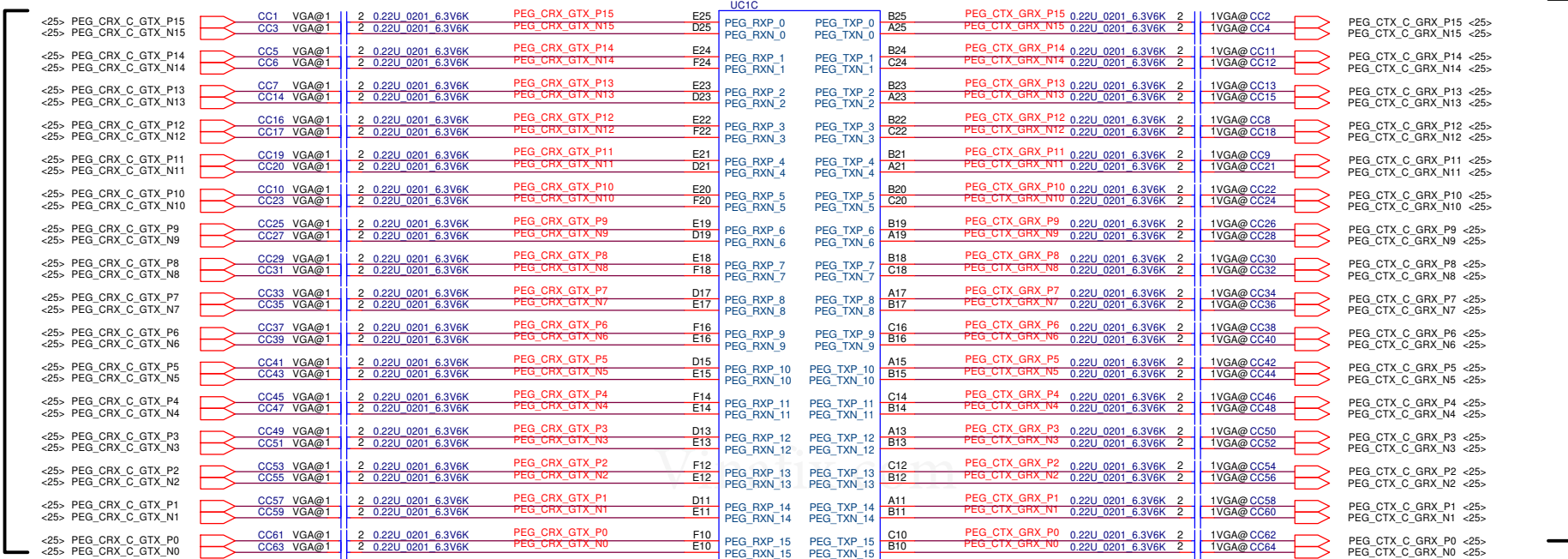


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PEG&DMI

To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed

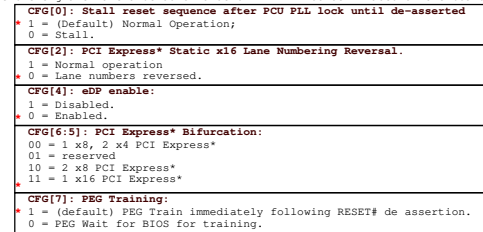


To PCH

To PCH

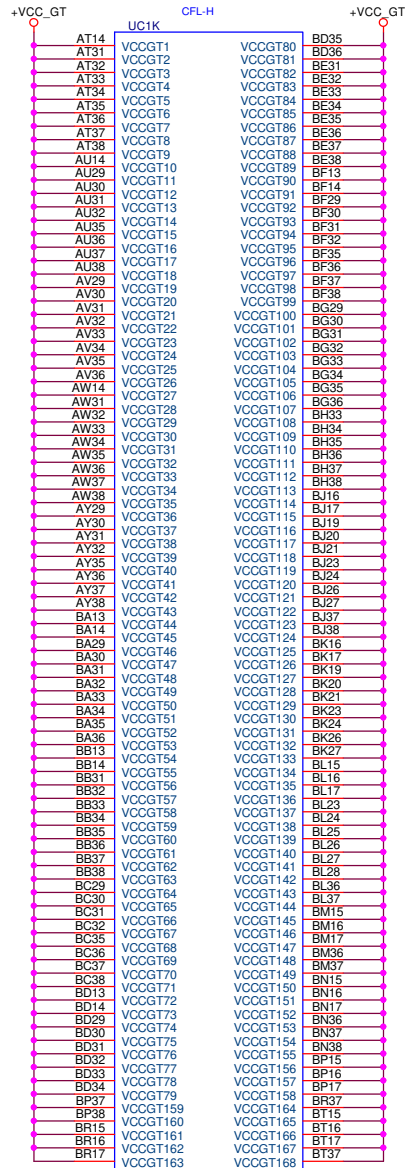


CFL-H_BGA1440



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GT
32000mA (Hexa Core GT2)



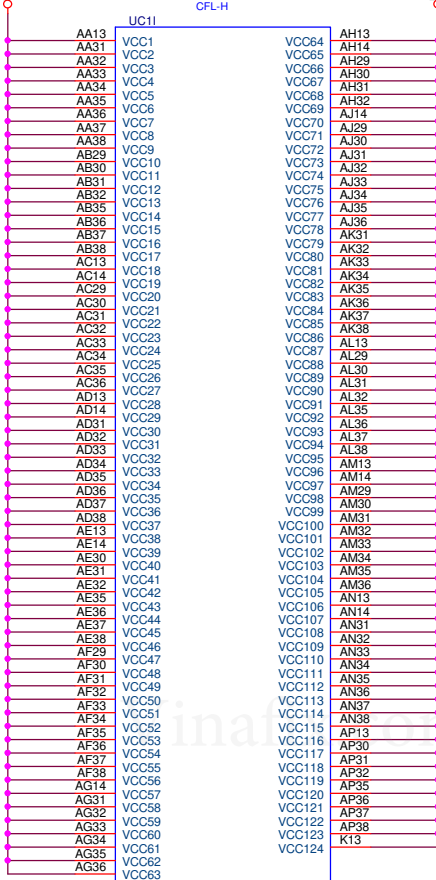
CFL-H_BGA1440
@

1. VccGT_Sense / VssGT_Sense Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

+VCC_CORE

CFL-H

+VCC_CORE



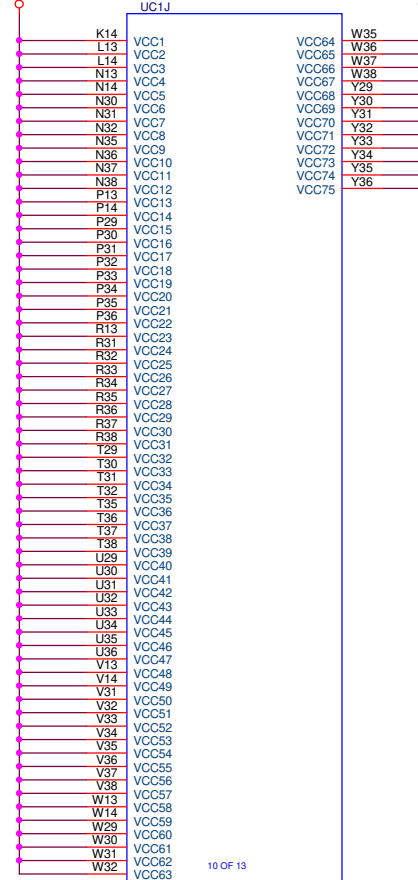
CFL-H_BGA1440
@

1. Vcc_SENSE / Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

+VCC_CORE

CFL-H

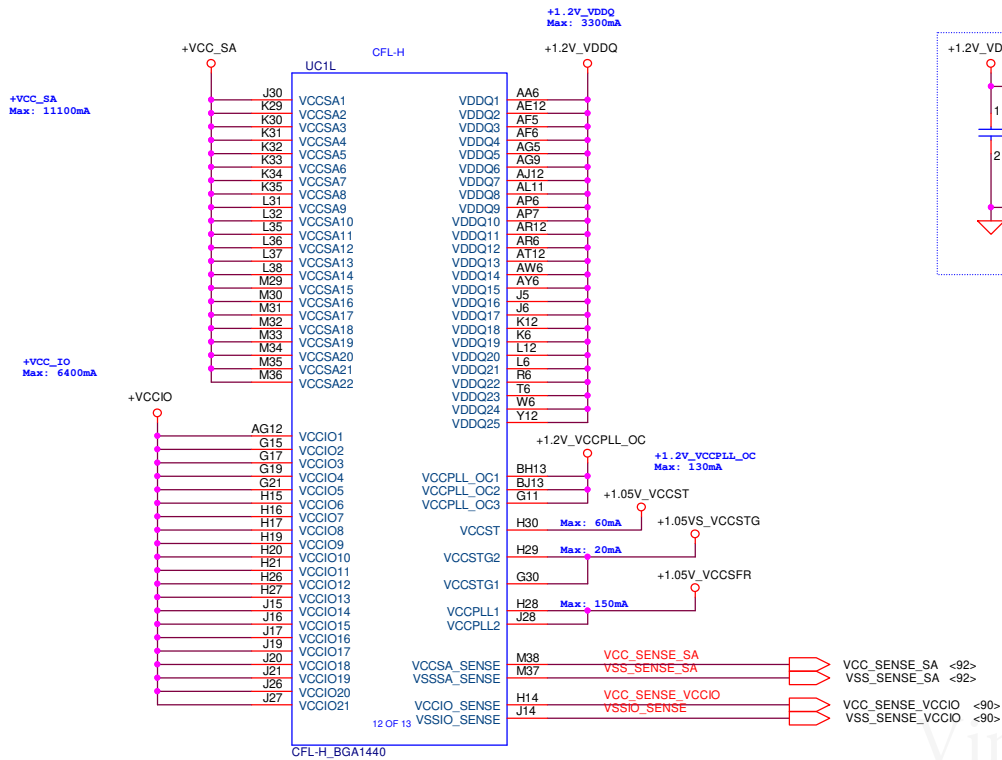
+VCC_CORE



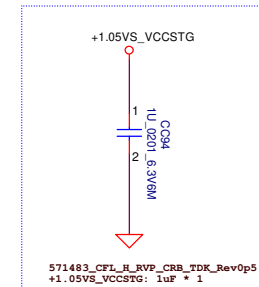
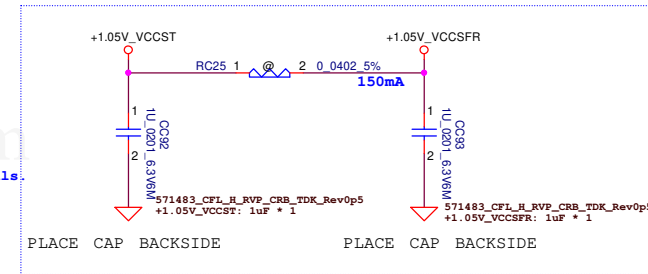
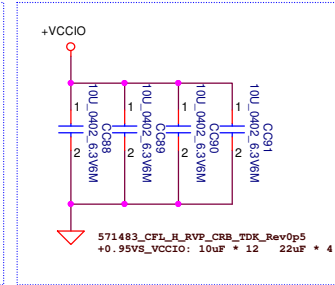
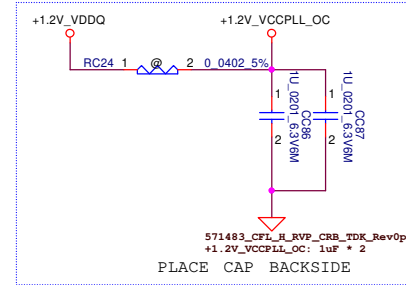
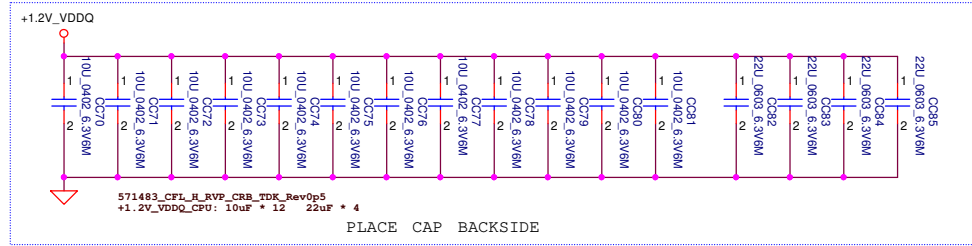
CFL-H_BGA1440
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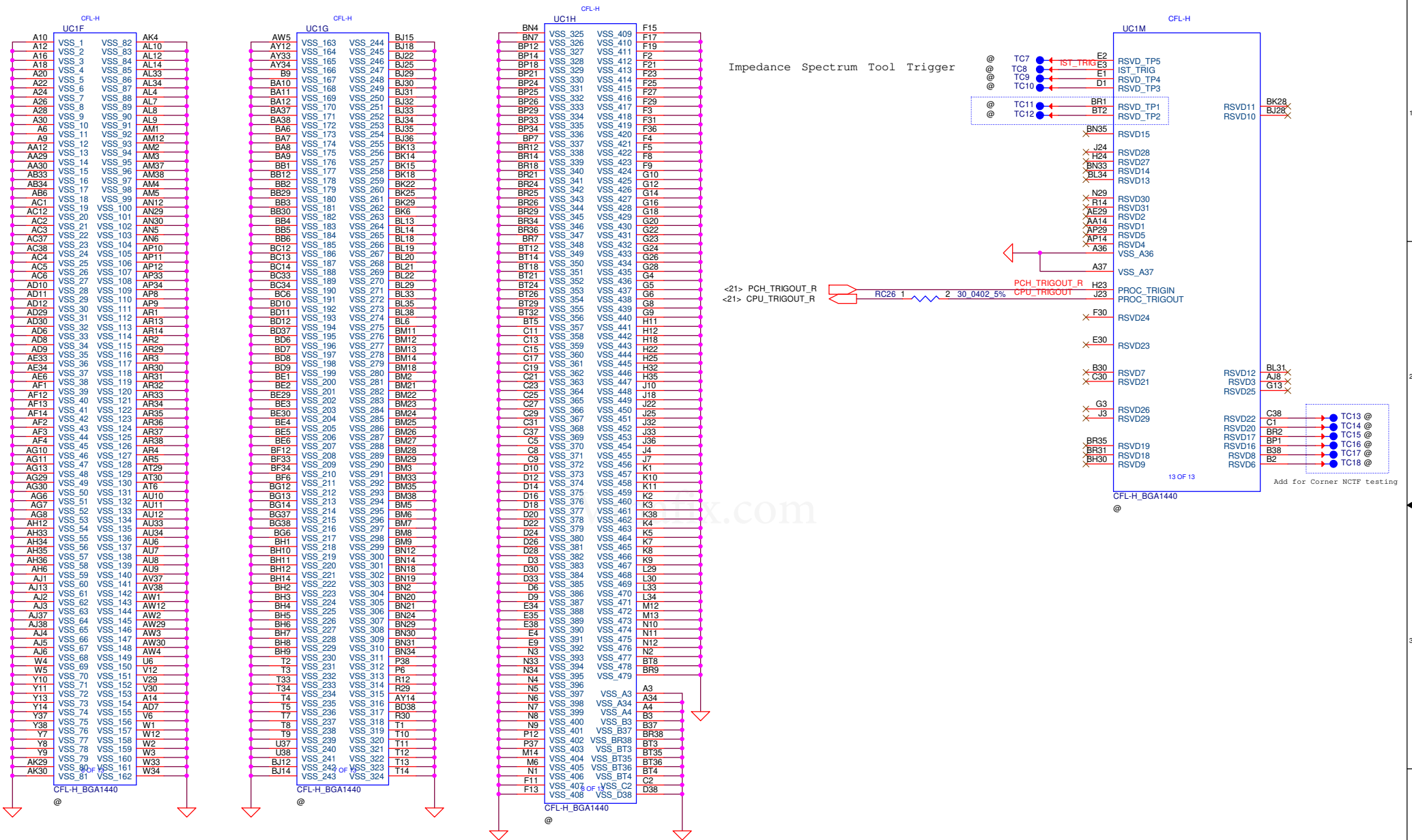
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						Size		Document Number		Rev	
						Custom		FH51M M/B LA-J871P		0.1	
						Date:		Wednesday, February 26, 2020		Sheet 11 of 112	

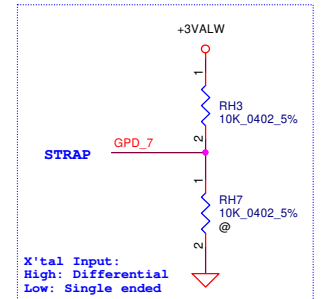
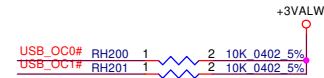
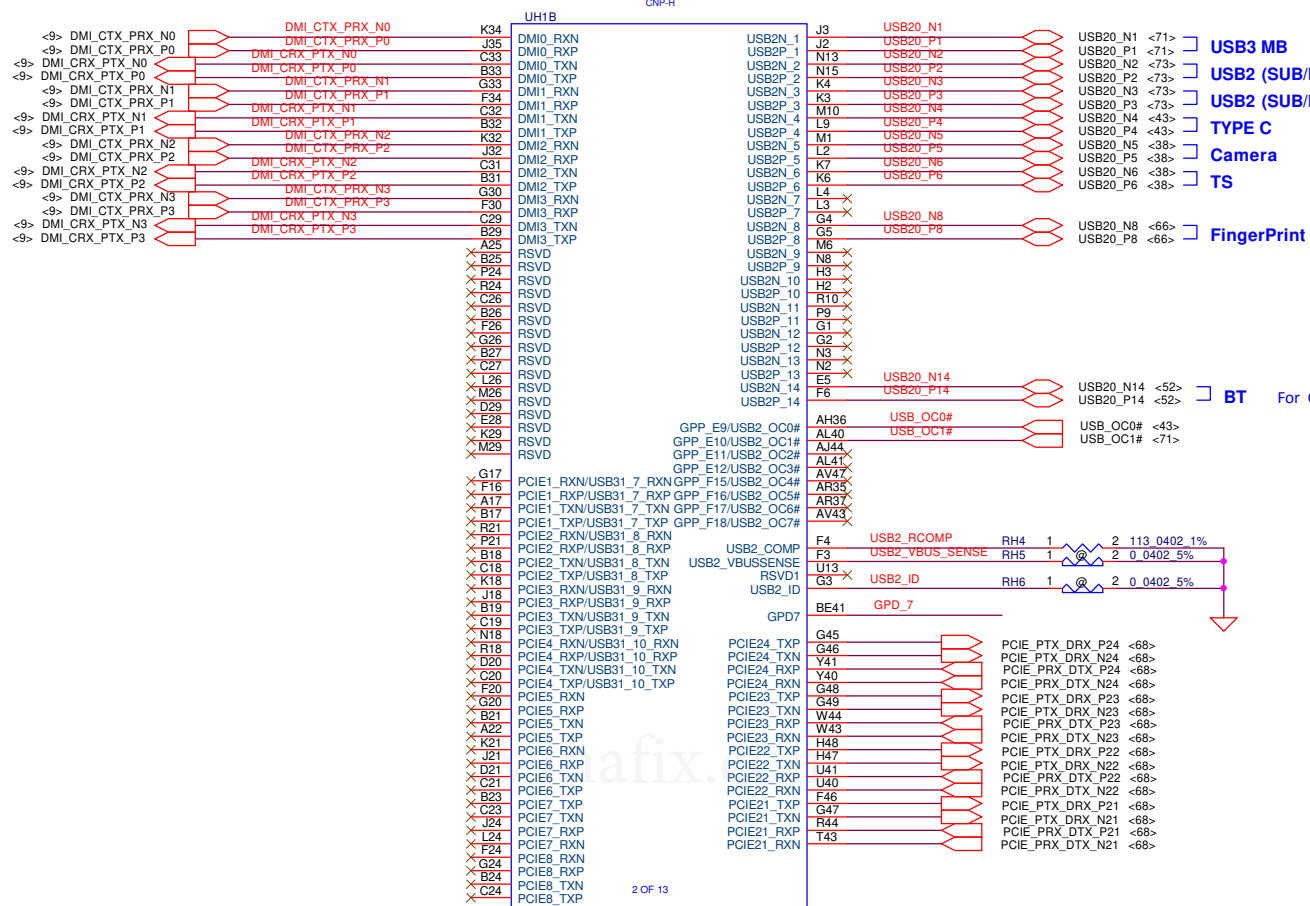


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	CFL-H(7/8)VCCSA/VCCIO/VDDQ
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				Custom	FH51M M/B LA-J871P
				Date:	Wednesday, February 26, 2020
				Sheet	12 of 112
				Rev	0.1





The 30 HSDIO lanes on PCH-H supports the following configurations:

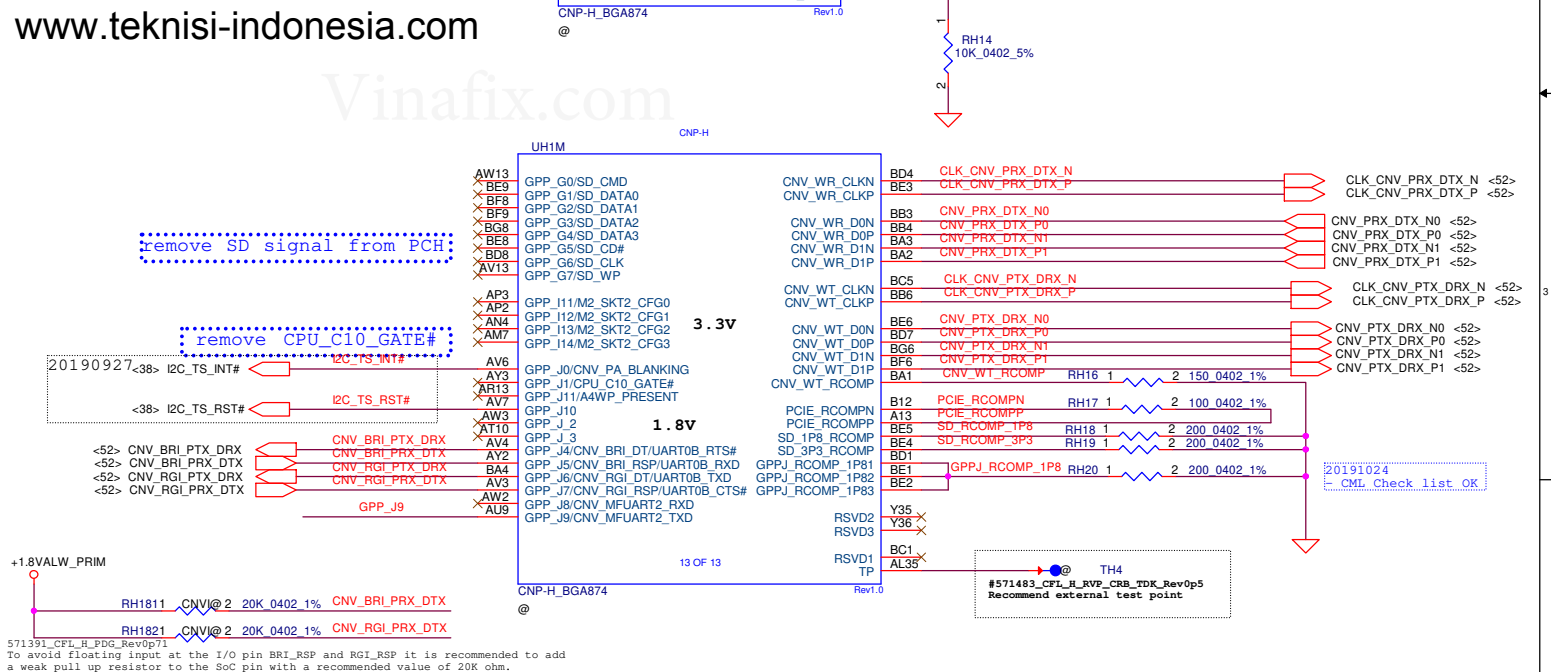
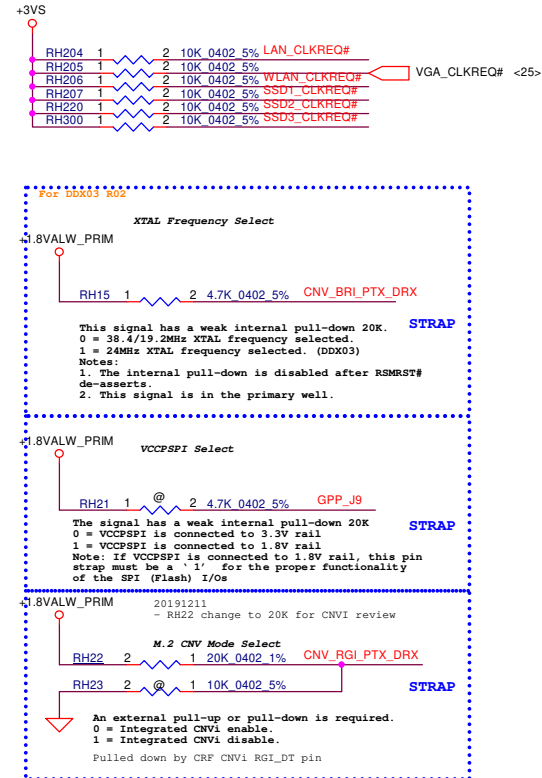
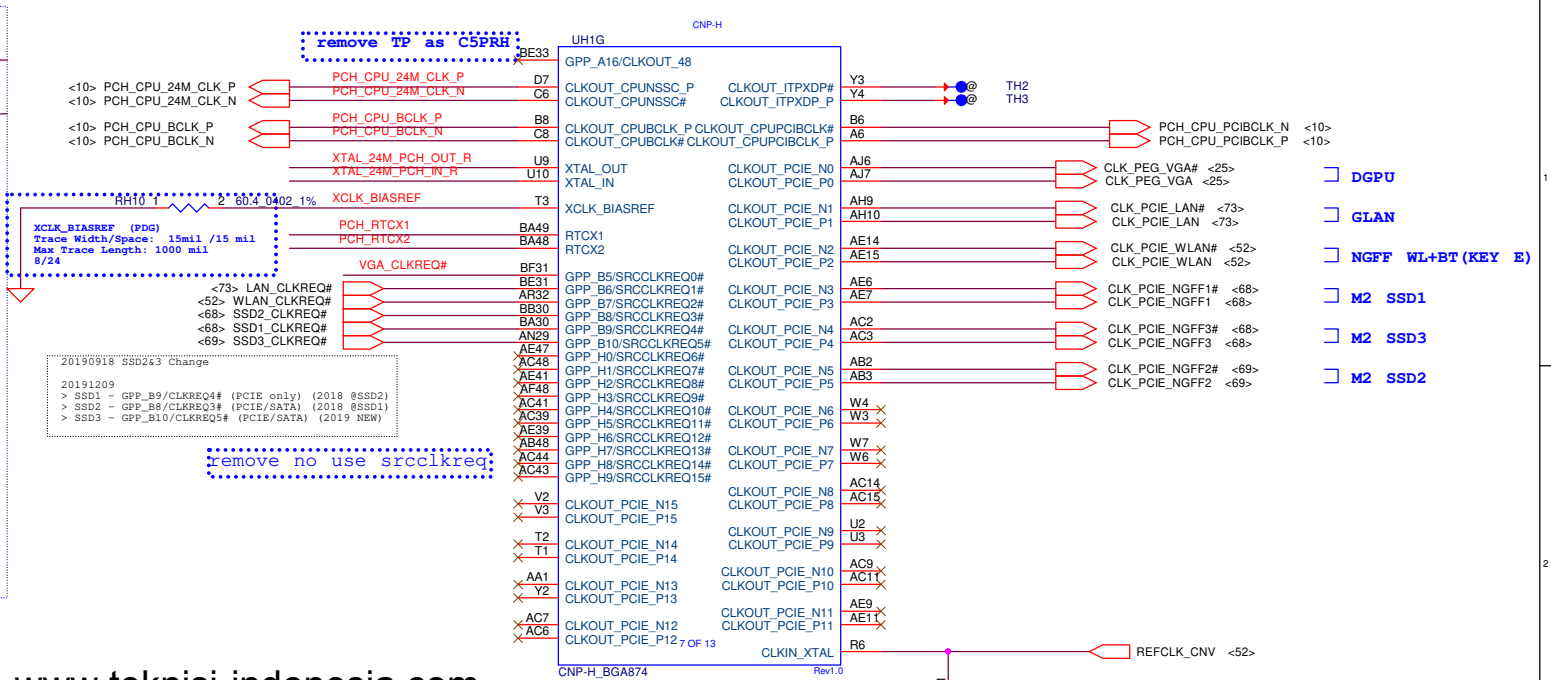
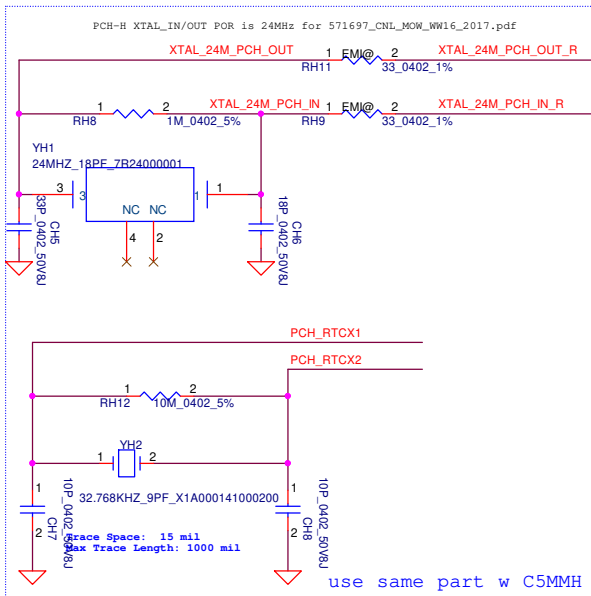
- Up to 24 PCIe* Lanes
 - A maximum of 16 PCIe* Ports (or devices) can be enabled
 - When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
 - Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
 - PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
- Up to 6 SATA Lanes
 - A maximum of 6 SATA Ports (or devices) can be enabled
 - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
 - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
 - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 GbE Lanes
 - A maximum of 1 GbE Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
 - x2 and x4 PCIe* NVMe SSD
 - x2 Intel® Optane® Memory Device
 - See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configurations, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support
- For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

HSIO Lane Assignments – Comet Lake PCH-H

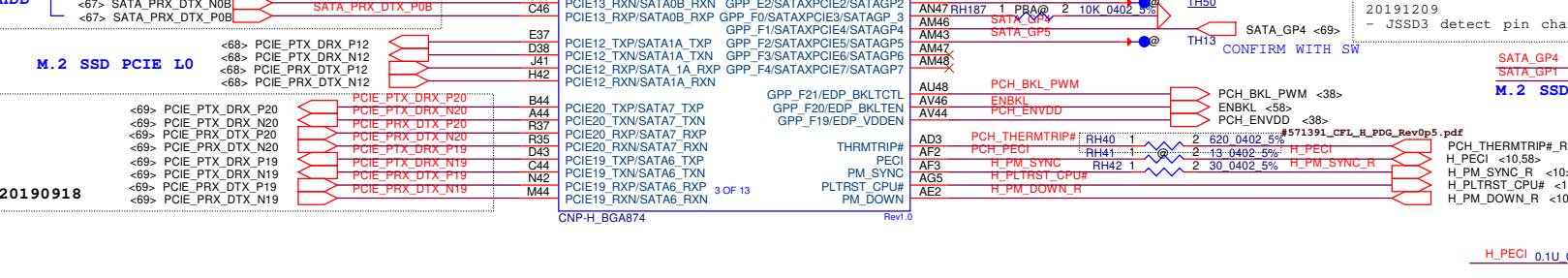
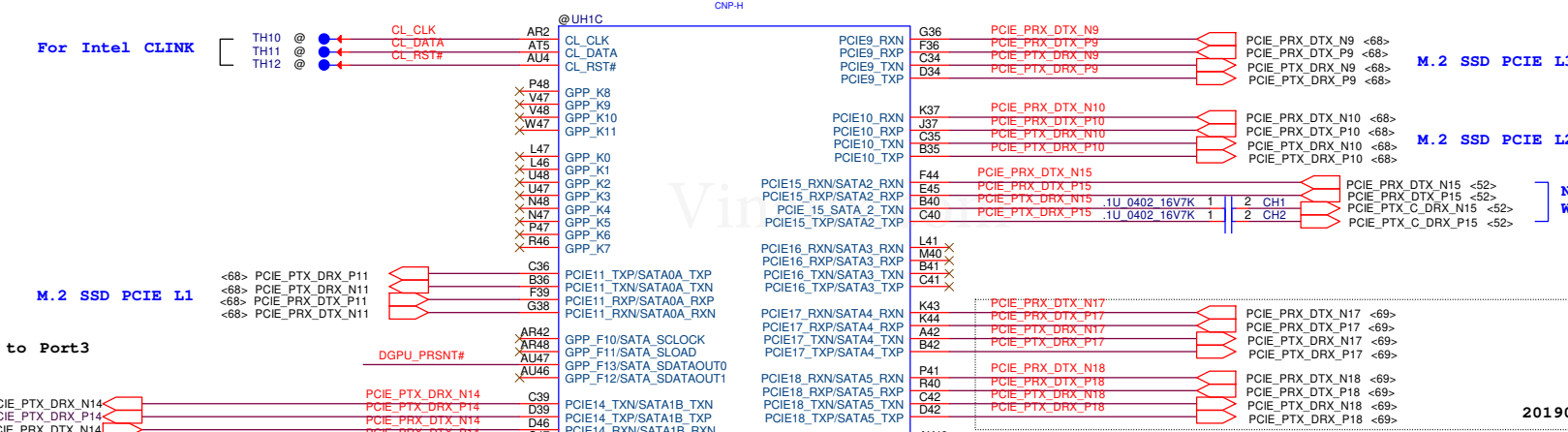
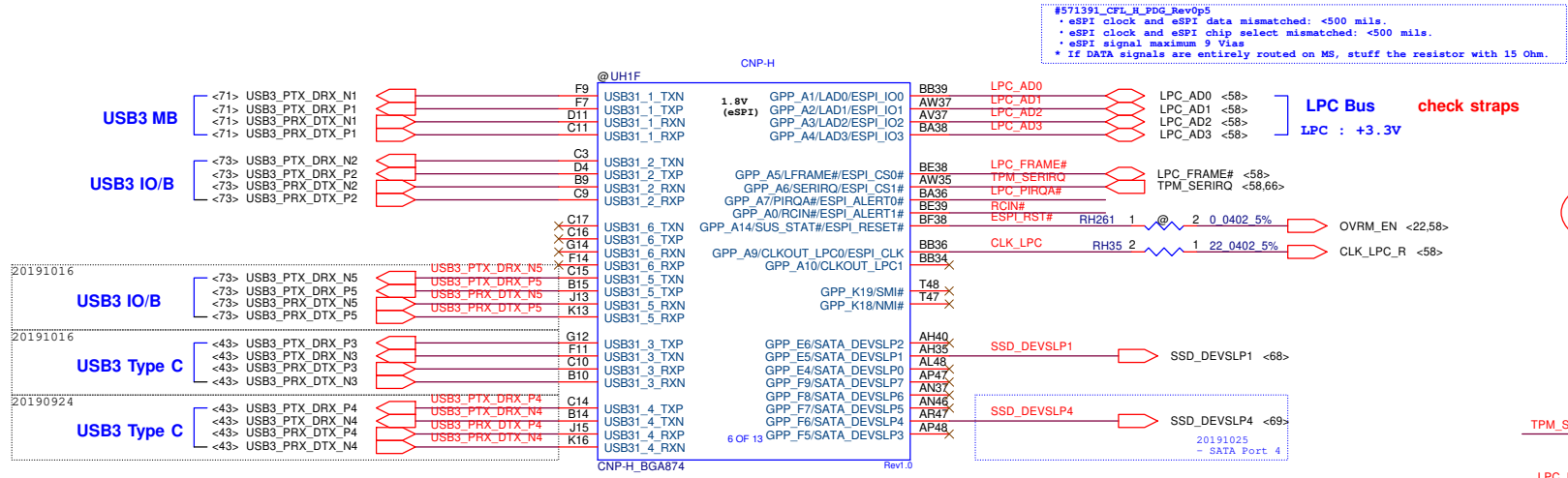
Lane	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30																																																																																													
Assignment	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30																																																																																													
Configuration	No Remapping						No Remapping						No Remapping						No Remapping						No Remapping																																																																																																		
SKU	<table><tr><td>H9470</td><td>USB 3.1 Gen 1 (10/10/1)</td><td>USB 3.1 Gen 1 (10/10/2)</td><td>USB 3.1 Gen 1 (10/10/3)</td><td>USB 3.1 Gen 1 (10/10/4)</td><td>USB 3.1 Gen 1 (10/10/5)</td><td>USB 3.1 Gen 1 (10/10/6)</td><td>USB 3.1 Gen 1 (10/10/7)</td><td>USB 3.1 Gen 1 (10/10/8)</td><td>USB 3.1 Gen 1 (10/10/9)</td><td>USB 3.1 Gen 1 (10/10/10)</td><td>PCIe 10.0/11</td><td>PCIe 10.0/12</td><td>PCIe 10.0/13</td><td>PCIe 10.0/14</td><td>PCIe 10.0/15</td><td>PCIe 10.0/16</td><td>PCIe 10.0/17</td><td>PCIe 10.0/18</td><td>PCIe 10.0/19</td><td>PCIe 10.0/20</td><td>PCIe 10.0/21</td><td>PCIe 10.0/22</td><td>PCIe 10.0/23</td><td>PCIe 10.0/24</td><td>PCIe 10.0/25</td><td>PCIe 10.0/26</td><td>PCIe 10.0/27</td><td>PCIe 10.0/28</td><td>PCIe 10.0/29</td><td>PCIe 10.0/30</td></tr><tr><td>H9470</td><td>USB 3.1 Gen 1 (10/10/1)</td><td>USB 3.1 Gen 1 (10/10/2)</td><td>USB 3.1 Gen 1 (10/10/3)</td><td>USB 3.1 Gen 1 (10/10/4)</td><td>USB 3.1 Gen 1 (10/10/5)</td><td>USB 3.1 Gen 1 (10/10/6)</td><td>USB 3.1 Gen 1 (10/10/7)</td><td>USB 3.1 Gen 1 (10/10/8)</td><td>USB 3.1 Gen 1 (10/10/9)</td><td>USB 3.1 Gen 1 (10/10/10)</td><td>PCIe 10.0/11</td><td>PCIe 10.0/12</td><td>PCIe 10.0/13</td><td>PCIe 10.0/14</td><td>PCIe 10.0/15</td><td>PCIe 10.0/16</td><td>PCIe 10.0/17</td><td>PCIe 10.0/18</td><td>PCIe 10.0/19</td><td>PCIe 10.0/20</td><td>PCIe 10.0/21</td><td>PCIe 10.0/22</td><td>PCIe 10.0/23</td><td>PCIe 10.0/24</td><td>PCIe 10.0/25</td><td>PCIe 10.0/26</td><td>PCIe 10.0/27</td><td>PCIe 10.0/28</td><td>PCIe 10.0/29</td><td>PCIe 10.0/30</td></tr><tr><td>H9470</td><td>USB 3.1 Gen 1 (10/10/1)</td><td>USB 3.1 Gen 1 (10/10/2)</td><td>USB 3.1 Gen 1 (10/10/3)</td><td>USB 3.1 Gen 1 (10/10/4)</td><td>USB 3.1 Gen 1 (10/10/5)</td><td>USB 3.1 Gen 1 (10/10/6)</td><td>USB 3.1 Gen 1 (10/10/7)</td><td>USB 3.1 Gen 1 (10/10/8)</td><td>USB 3.1 Gen 1 (10/10/9)</td><td>USB 3.1 Gen 1 (10/10/10)</td><td>PCIe 10.0/11</td><td>PCIe 10.0/12</td><td>PCIe 10.0/13</td><td>PCIe 10.0/14</td><td>PCIe 10.0/15</td><td>PCIe 10.0/16</td><td>PCIe 10.0/17</td><td>PCIe 10.0/18</td><td>PCIe 10.0/19</td><td>PCIe 10.0/20</td><td>PCIe 10.0/21</td><td>PCIe 10.0/22</td><td>PCIe 10.0/23</td><td>PCIe 10.0/24</td><td>PCIe 10.0/25</td><td>PCIe 10.0/26</td><td>PCIe 10.0/27</td><td>PCIe 10.0/28</td><td>PCIe 10.0/29</td><td>PCIe 10.0/30</td></tr></table>																														H9470	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30	H9470	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30	H9470	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30
H9470	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30																																																																																													
H9470	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30																																																																																													
H9470	USB 3.1 Gen 1 (10/10/1)	USB 3.1 Gen 1 (10/10/2)	USB 3.1 Gen 1 (10/10/3)	USB 3.1 Gen 1 (10/10/4)	USB 3.1 Gen 1 (10/10/5)	USB 3.1 Gen 1 (10/10/6)	USB 3.1 Gen 1 (10/10/7)	USB 3.1 Gen 1 (10/10/8)	USB 3.1 Gen 1 (10/10/9)	USB 3.1 Gen 1 (10/10/10)	PCIe 10.0/11	PCIe 10.0/12	PCIe 10.0/13	PCIe 10.0/14	PCIe 10.0/15	PCIe 10.0/16	PCIe 10.0/17	PCIe 10.0/18	PCIe 10.0/19	PCIe 10.0/20	PCIe 10.0/21	PCIe 10.0/22	PCIe 10.0/23	PCIe 10.0/24	PCIe 10.0/25	PCIe 10.0/26	PCIe 10.0/27	PCIe 10.0/28	PCIe 10.0/29	PCIe 10.0/30																																																																																													

Intel® RST for PCIe Storage port configurable as M.2 x2/x4

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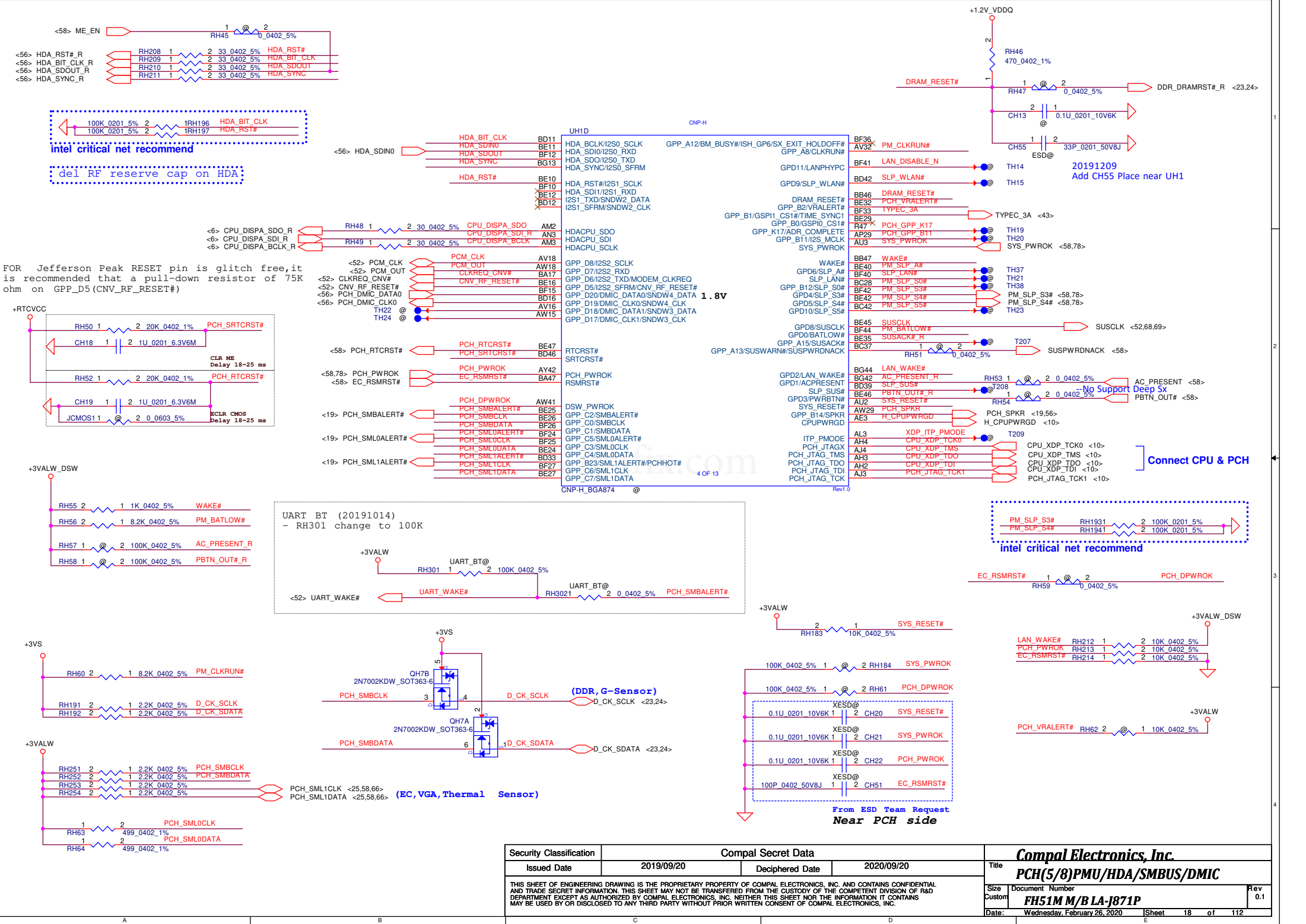
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				Size	Document Number		Rev
				Custom	FH51M M/B LA-871P		0.1
				Date:	Wednesday, February 26, 2020	Sheet	15 of 112

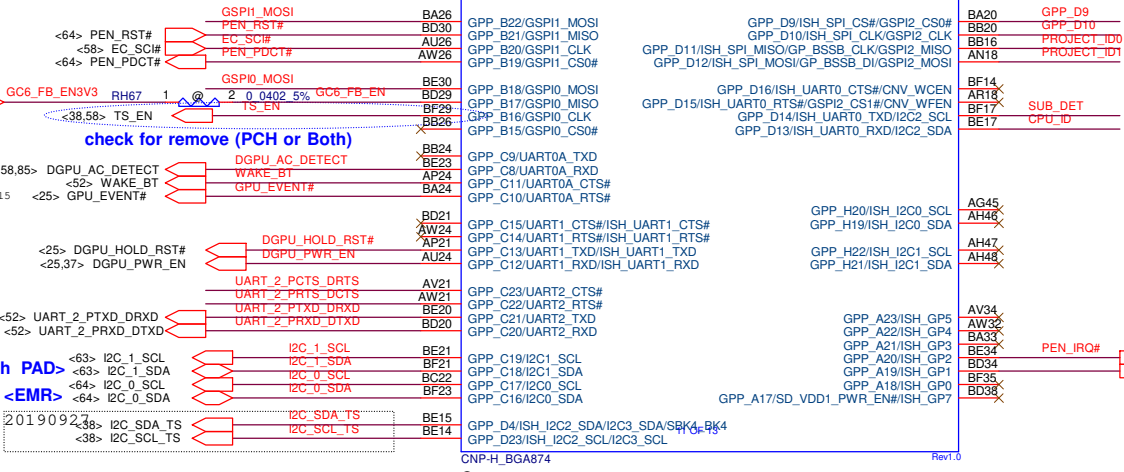
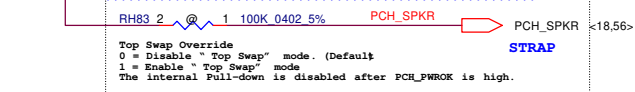
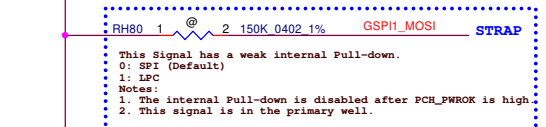
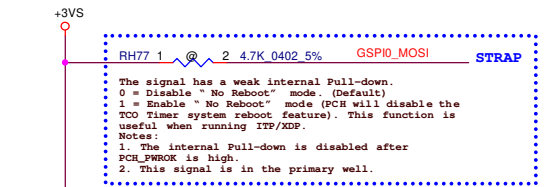
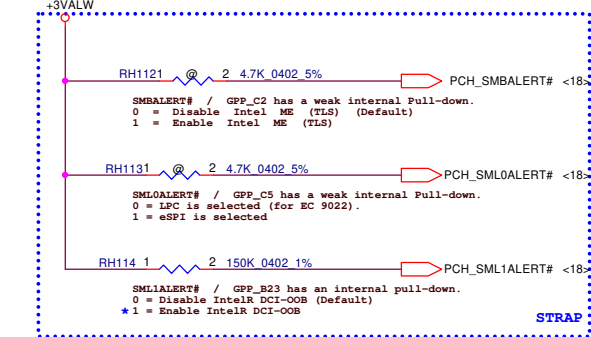
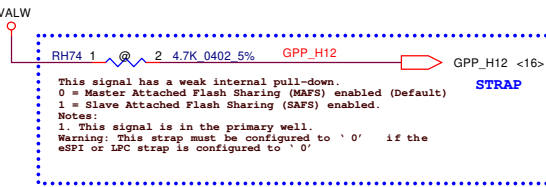
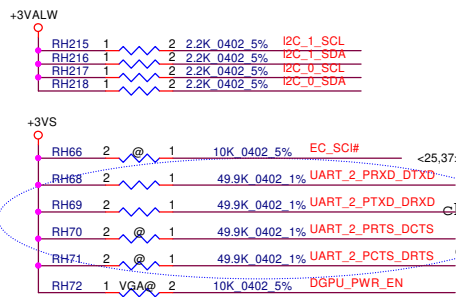


	GPP_F13
	DGPU_PRNST#
DIS,Optimus	0
UMA	1

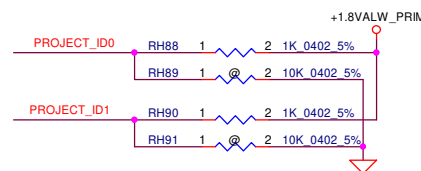
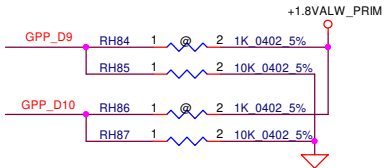
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Issued Date	2019/09/20	Deciphered Date	2020/09/20
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PCIE/SATA/USB3/eSPI	
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	GPP_D10	GPP_D9
Reserved	0	0
Reserved	0	1
Reserved	1	0
for 8 Layer	1	1

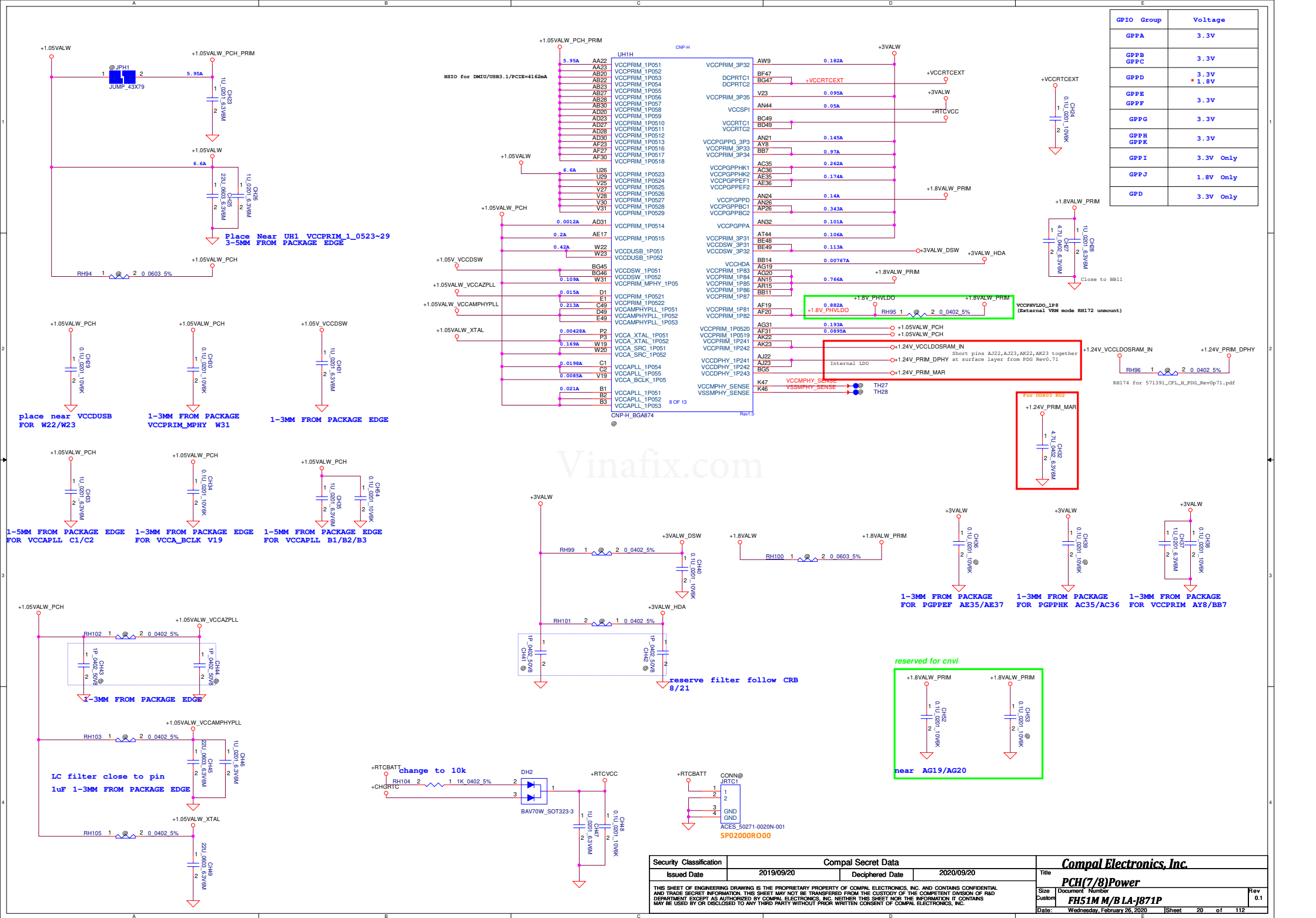
Project ID	Project ID1 GPP_D12	Project ID0 GPP_D11
A7	0	0
NA	0	1
2020 Gaming 50	1	0
*2020 Gaming 60	1	1

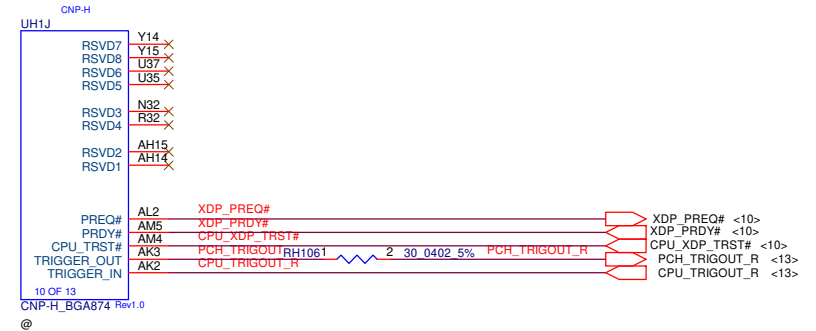
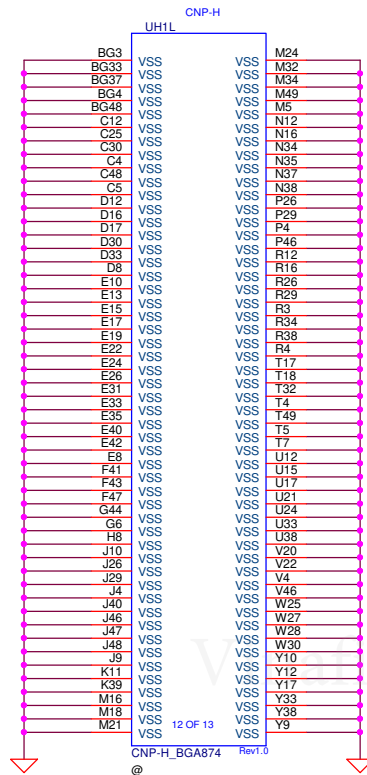
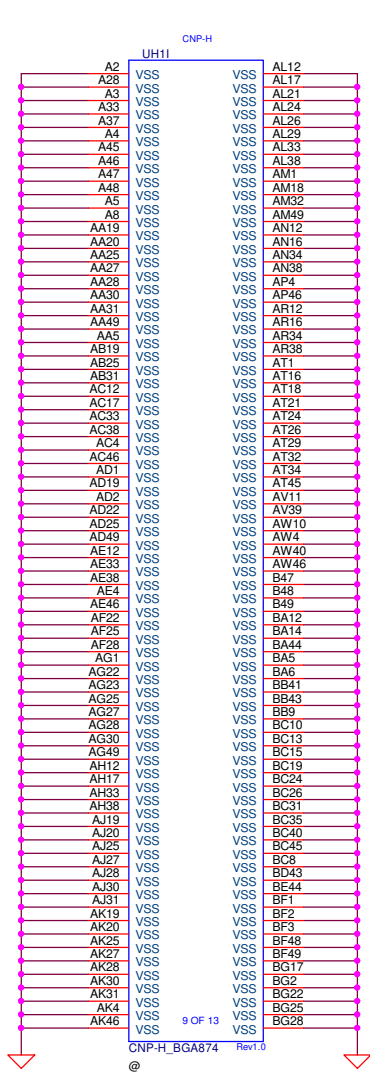
SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
• GPP_B14, GPP_B20, GPP_B23
• GPP_C[23:22]
• GPP_D[4:0]
• GPP_E[8:0]
• GPP_I[3:0]
• GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPP_G, (which are 3.3V only), and GPP_J group (which is 1.8V only).

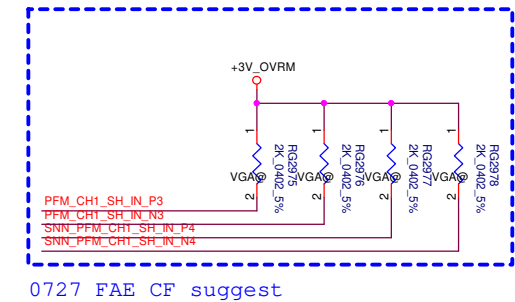
All GPIOs have programmable internal pull-up/pull-down resistors which are off by default. The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

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				Date:	Wednesday, February 26, 2020	Sheet 19 of 112

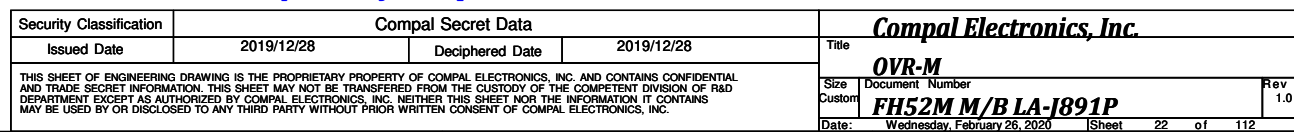




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				Custom	FH51M M/B LA-J871P
				Date:	Wednesday, February 26, 2020
				Sheet	21 of 112
				Rev	0.1



0730 FAE CF suggest ,
reserve pull high only



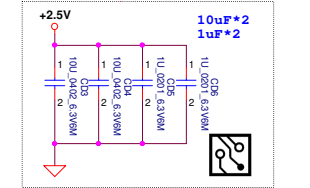
CHANNEL-A (Interleaved Memory)

> BOT : Reverse type (4mm)

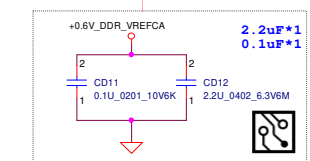
> Non-ECC SO-DIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

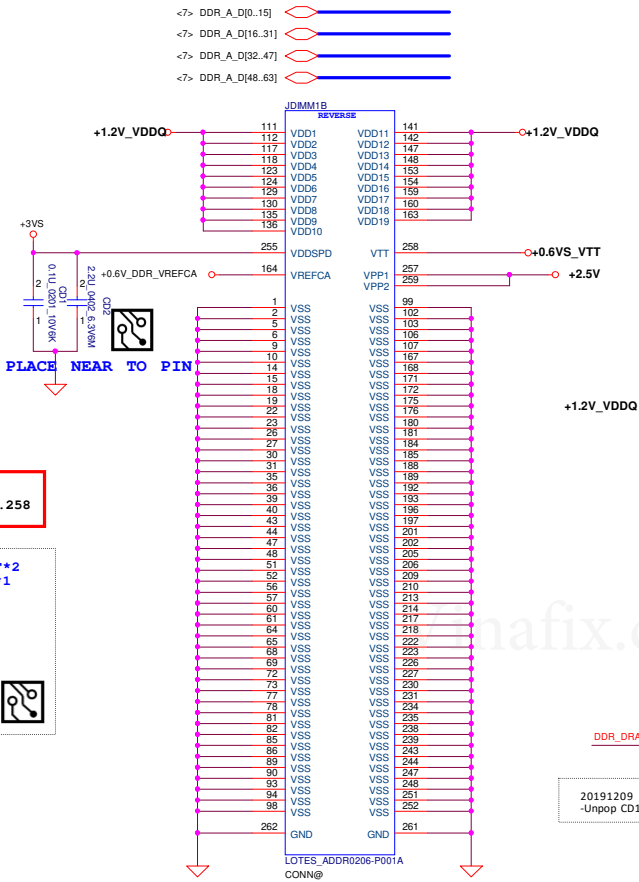
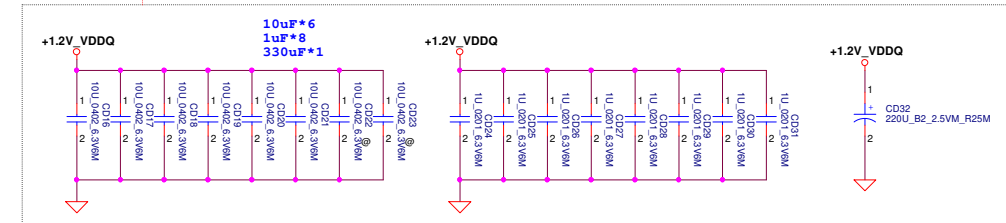
Layout Note:
Place near JDIMM1.257,259



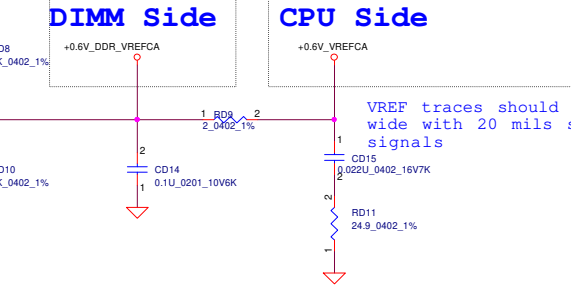
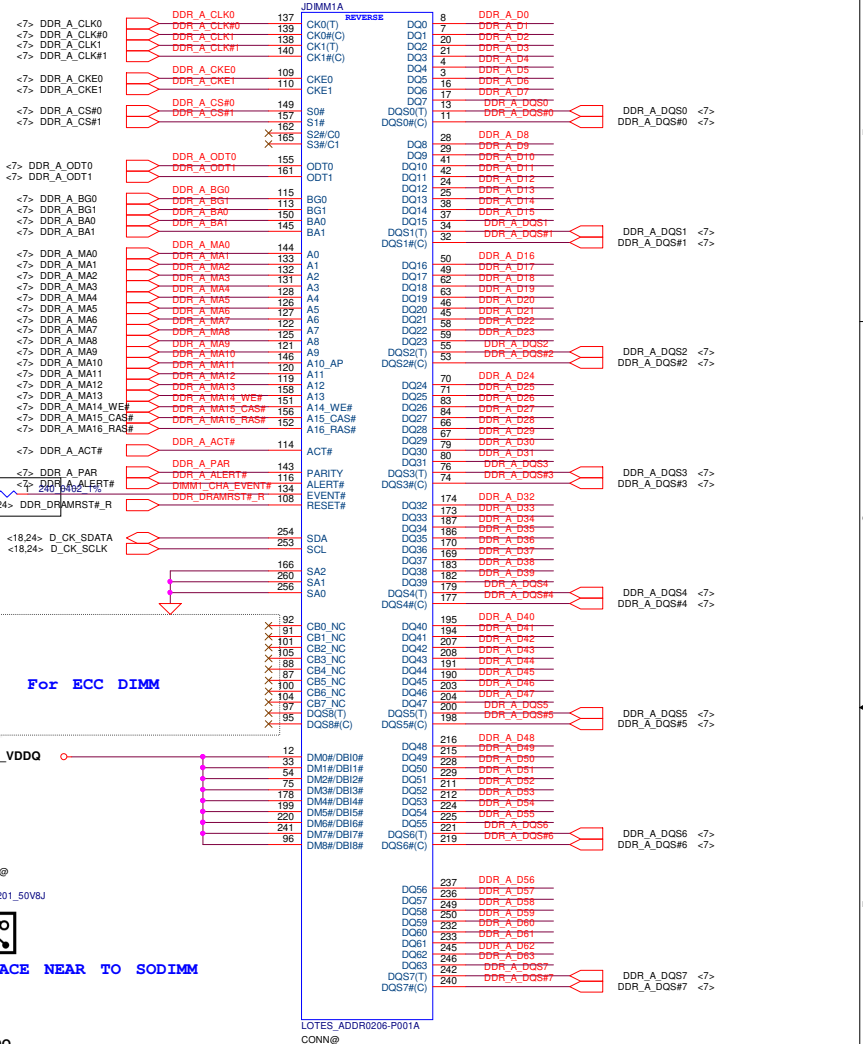
Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1



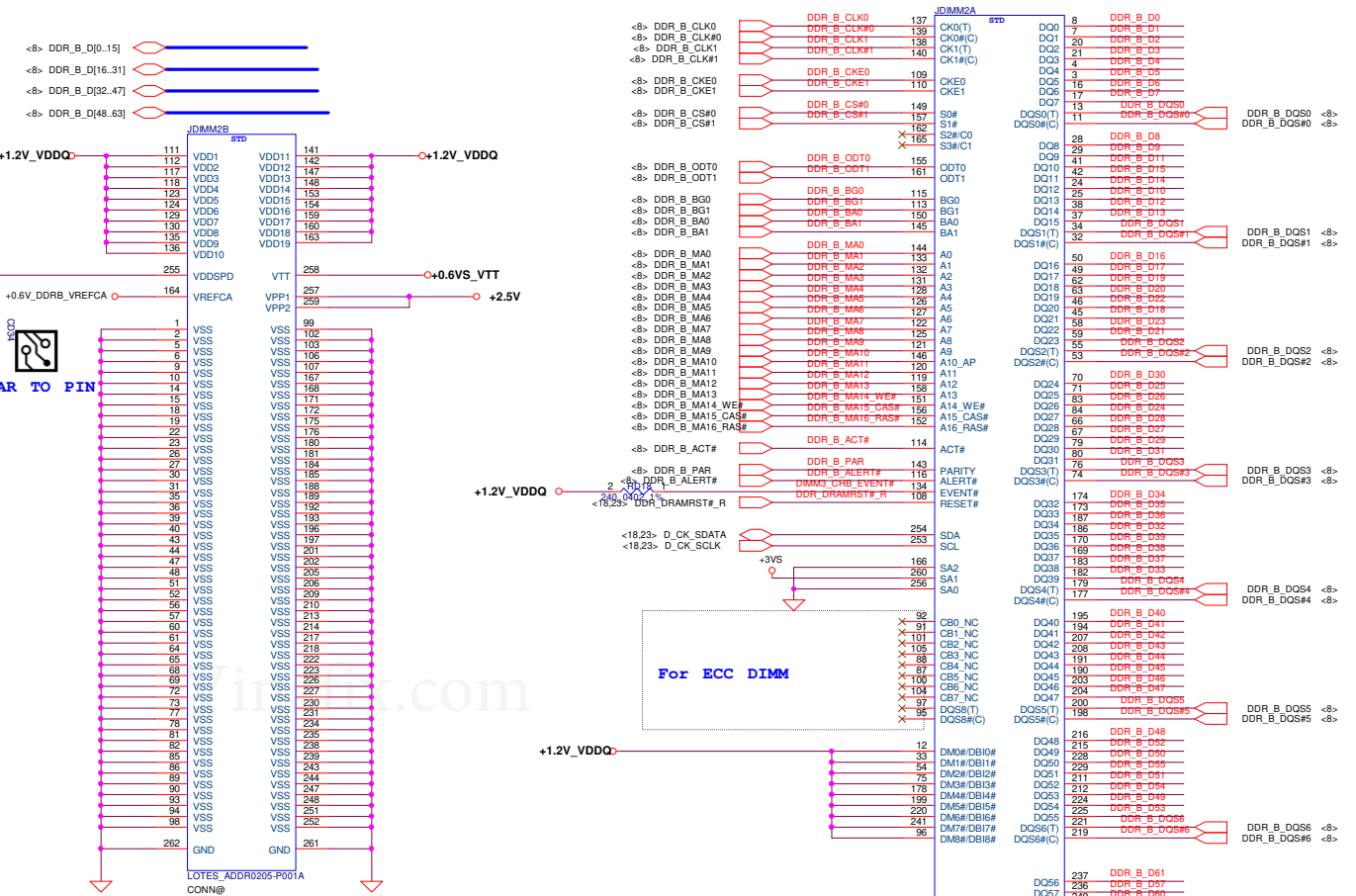
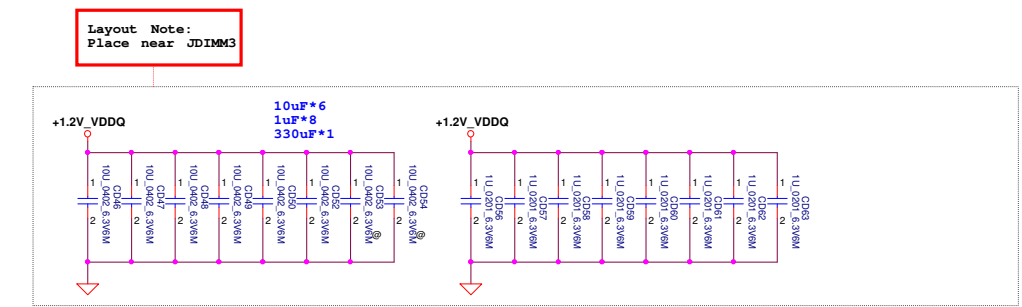
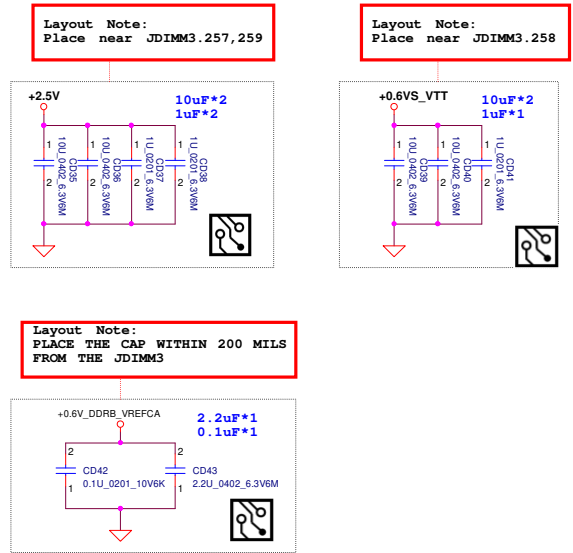
Part Number: SP07001CY00
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4



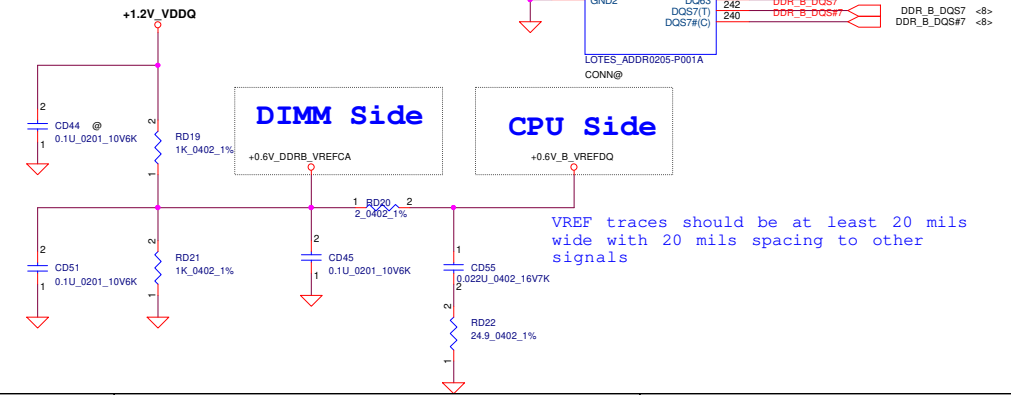
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

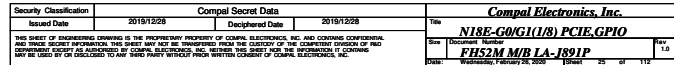
CHANNEL-B (Interleaved Memory)
> BOT : STD type (4mm)
> Non-ECC SO-DIMM

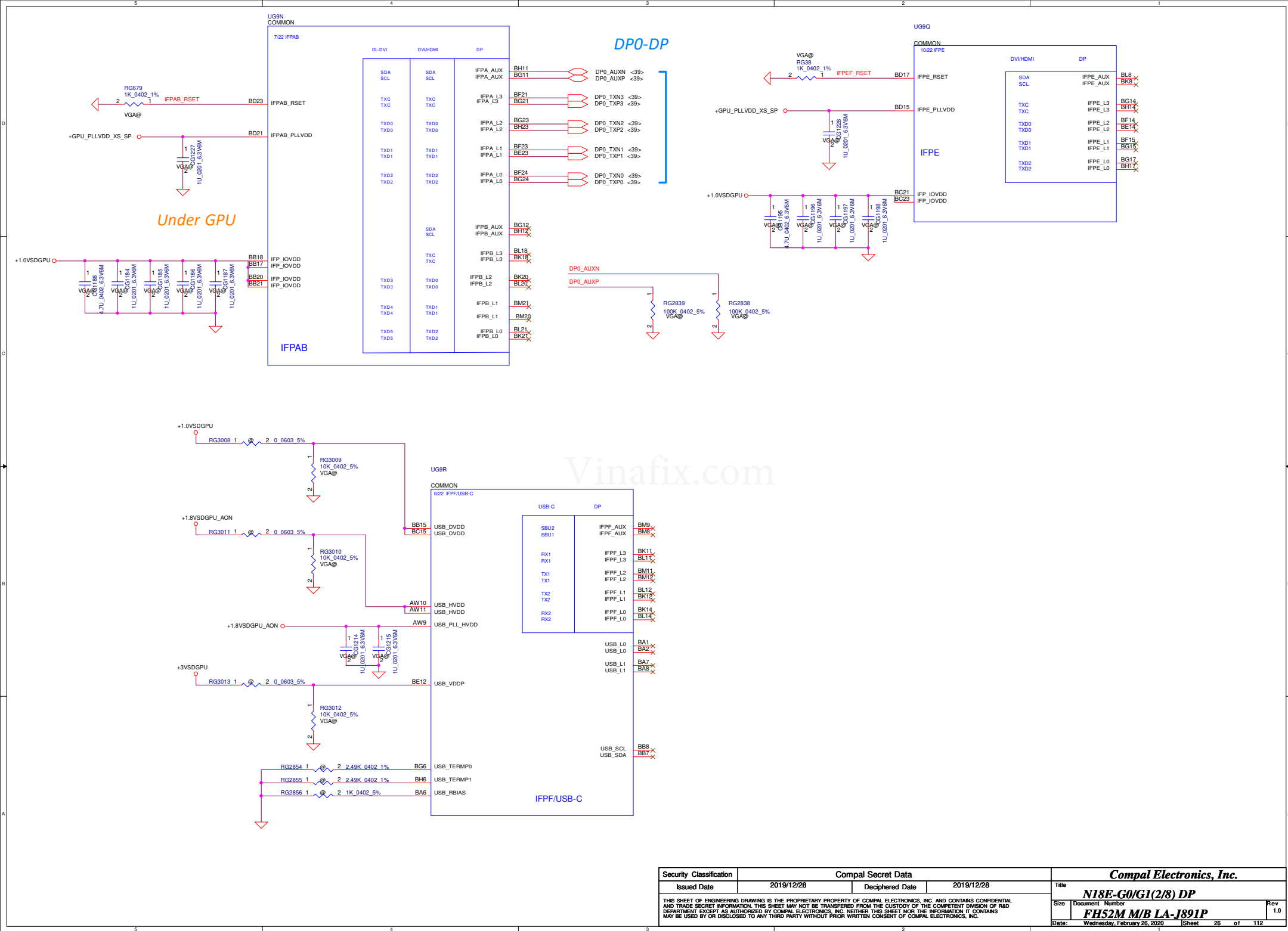
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



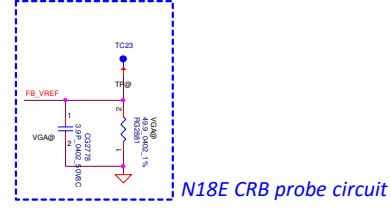
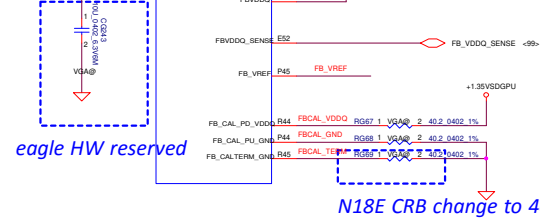
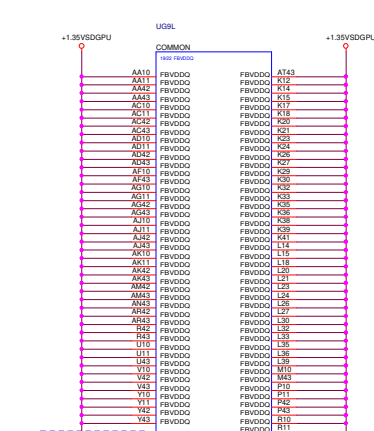
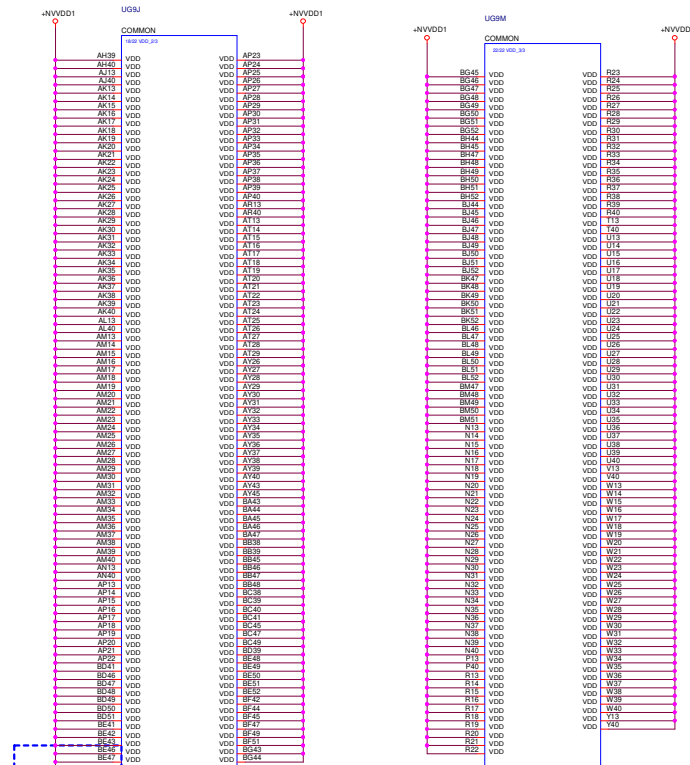
Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD



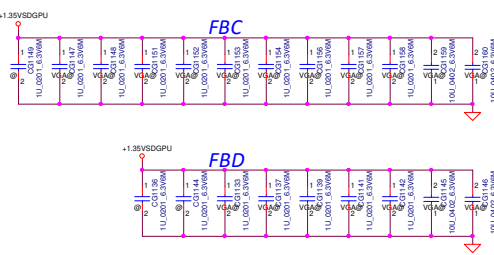
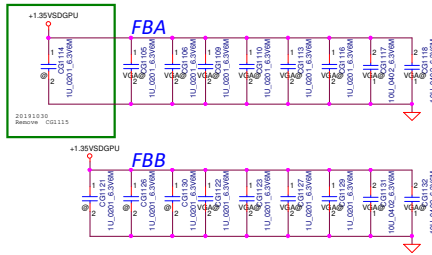
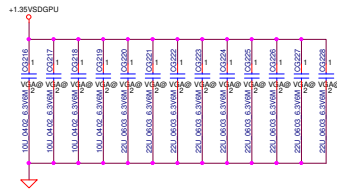




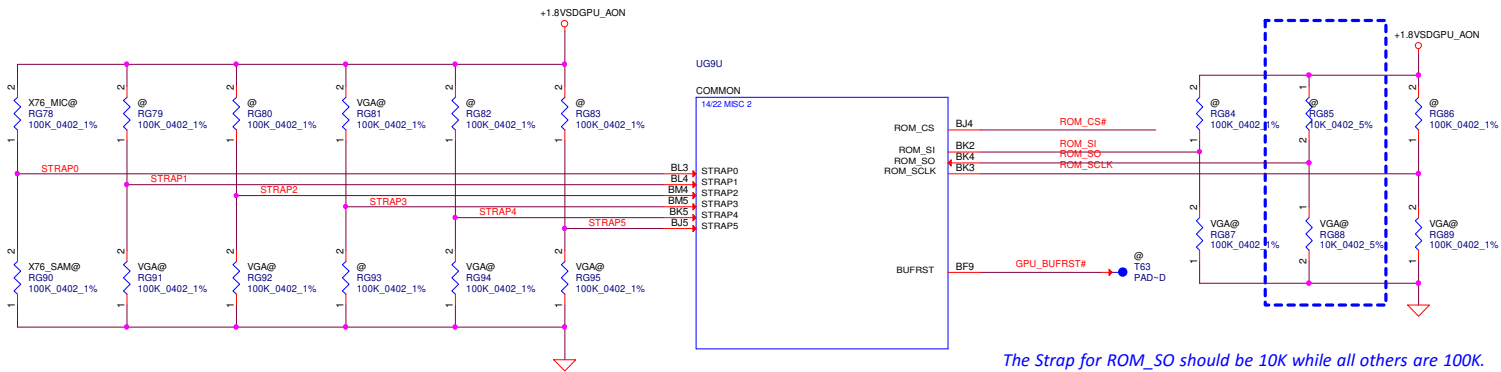




Place under GPU



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Issued Date	2019/12/28	Deciphered Date	2019/12/28	N18E-G0/G1(S18) Power	
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The Strap for ROM_SO should be 10K while all others are 100K.

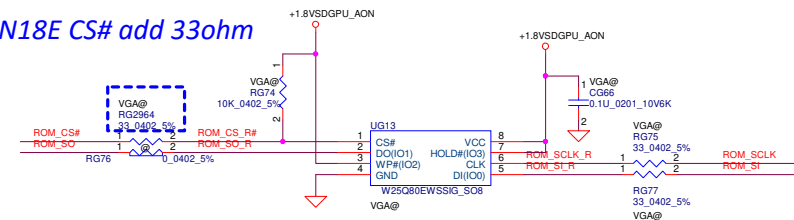
	(LSB)	(MSB)	(LSB)	(MSB)					
<i>G-sync with VGA device</i>	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	ROM_SO	ROM_SI	ROM_SCLK
Samsung K4Z80325BC-HC14	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm
MICRON MT61K256M32JE-14:A	PU 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm

Table 1. N18E-G3 GDDR6 Recommended Memories

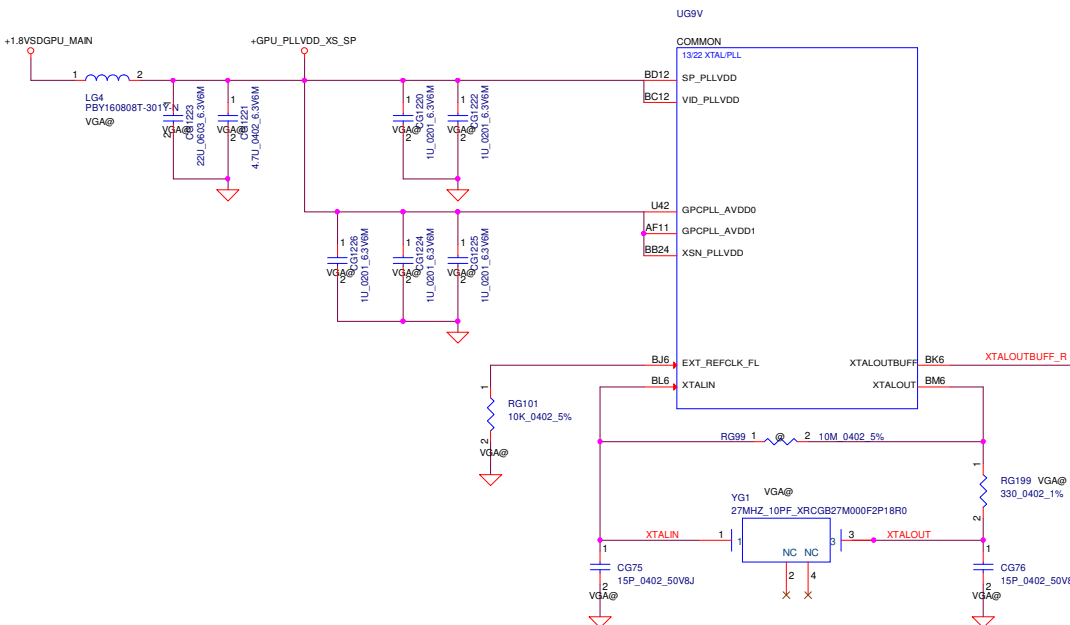
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Sheets	Memory Speed Grade	Date Code	RoHS	RoHS Plan	Status
8 Gb	2048x16x16 and 1.35V	1.35V	Micro	N18E-G3G6A32JE-14:A	1.4	0x0	14 Gbps	N/A	Full	Full	Production candidate

Notes:
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

N18E CS# add 33ohm



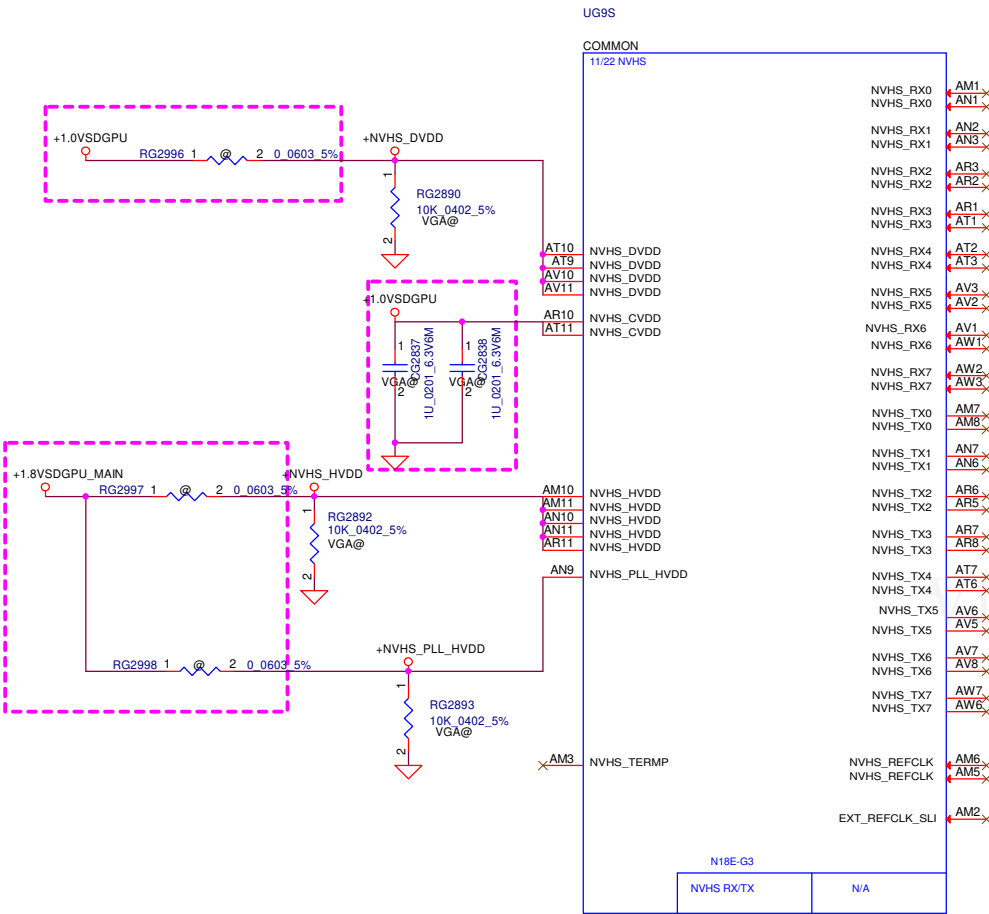
DGPU VBIOS ROM 8Mb
P/N : SA00009QP00



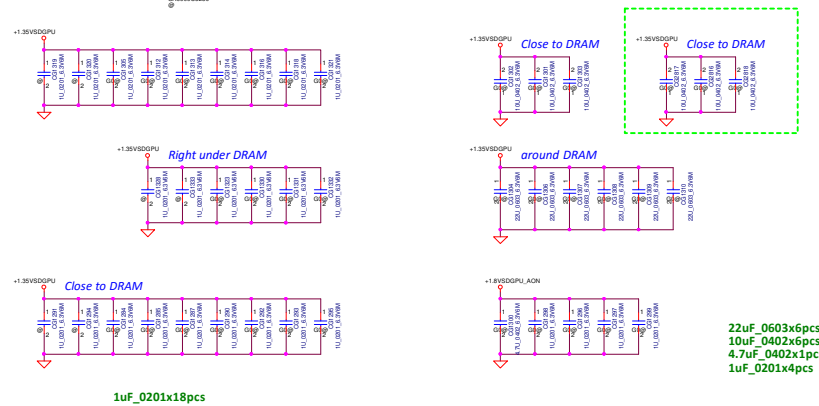
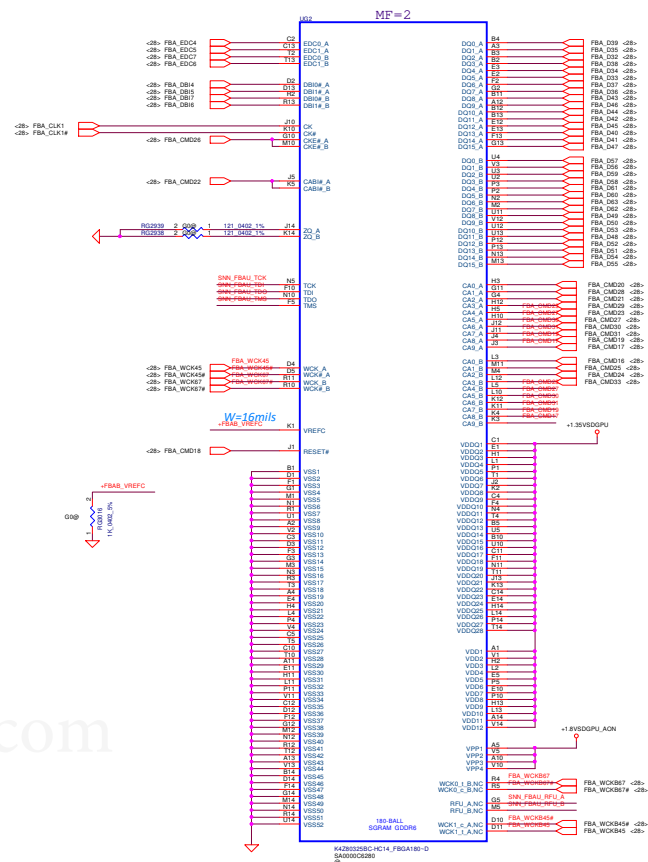
www.teknisi-indonesia.com

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Date: Wednesday, February 26, 2020				Sheet 31 of 112

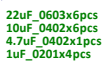
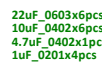
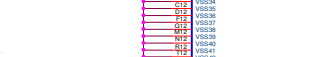
Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



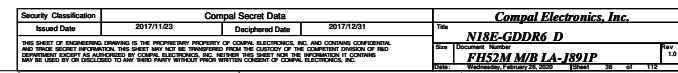
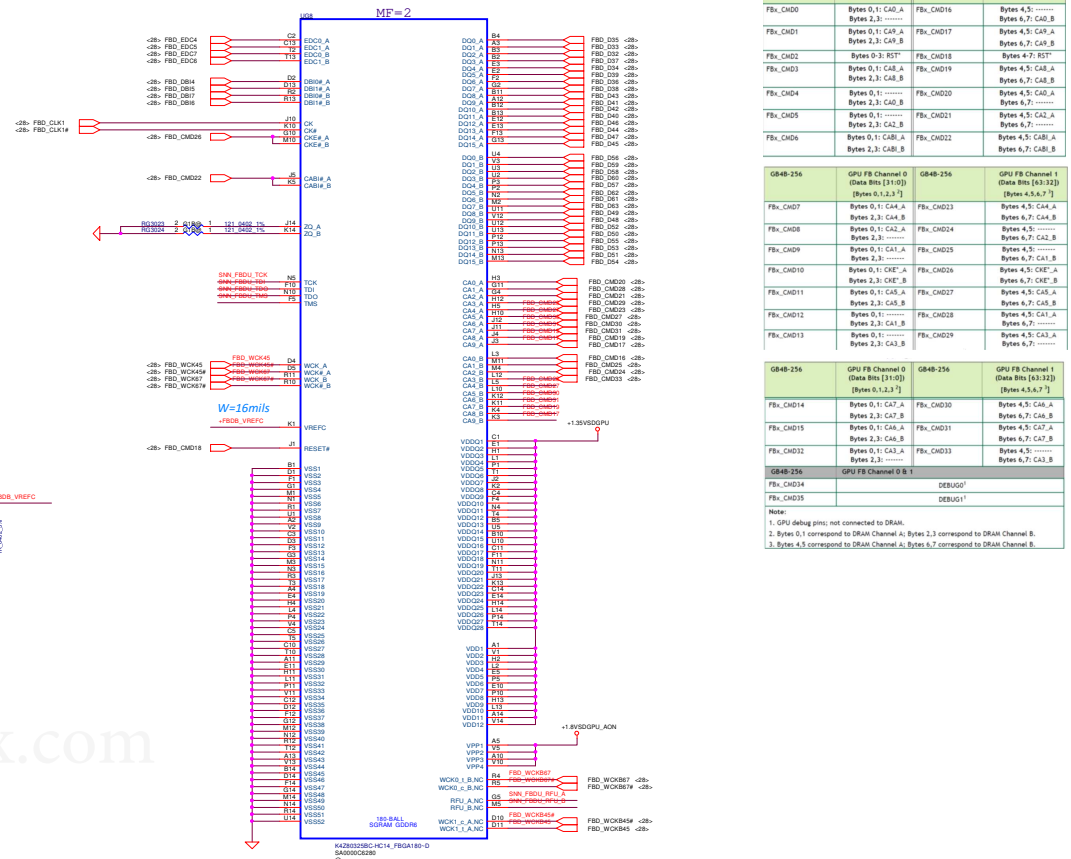
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Issued Date	2019/12/28	Deciphered Date	2019/12/28	Title	
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Size		Document Number			Rev
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Drawn	2019/12/28	Checked	2019/12/28	Rev
FHS2M M/B LA-1891P			33	1.0



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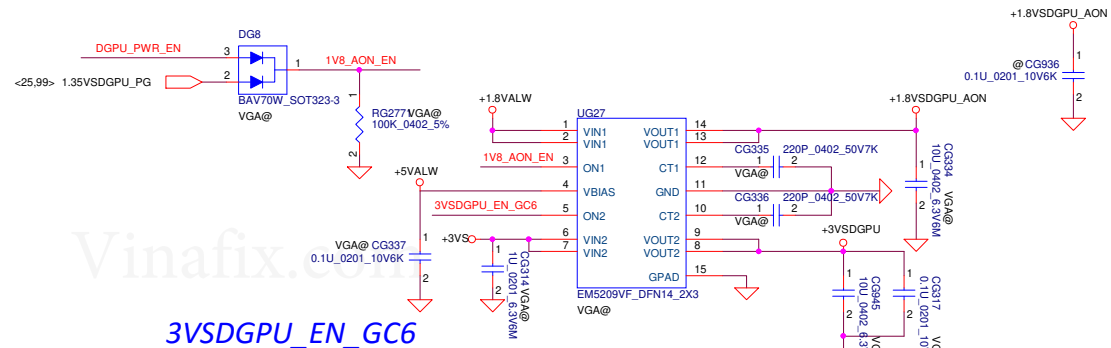
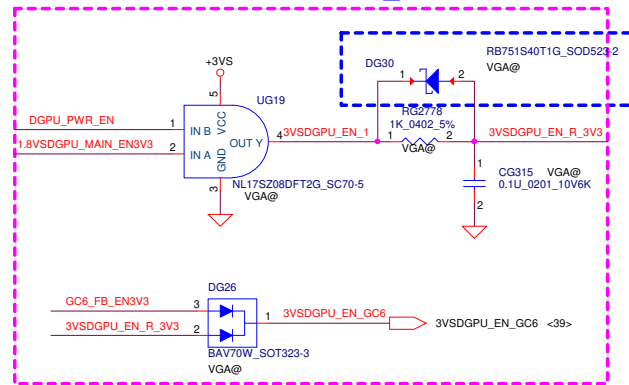
remove GPK

<19,25> DGPU_PWR_EN
<25,99> 1.35VSDGPU_EN
<25,101> NVVDD1_EN
<25> 1.8VSDGPU_MAIN_EN
<25> 1.8VSDGPU_MAIN_EN3V3
<19,25> GC6_FB_EN3V3
<25> OVERT#
<25> DGPU_PEX_RST#



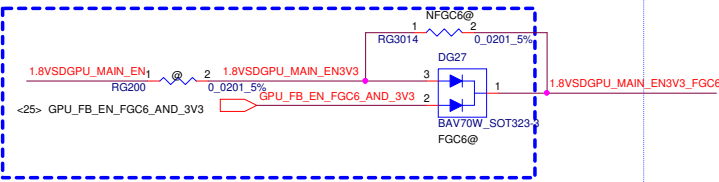
Reserve for 1.8V O.D. pin.

+1.8VALW to +1.8VSDGPU_AON & +3VS to +3VSDGPU

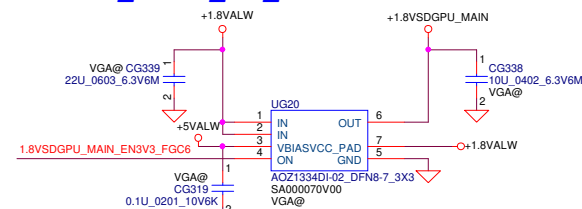


3VSDGPU_EN_GC6

+1.8VALW to +1.8VSDGPU_MAIN

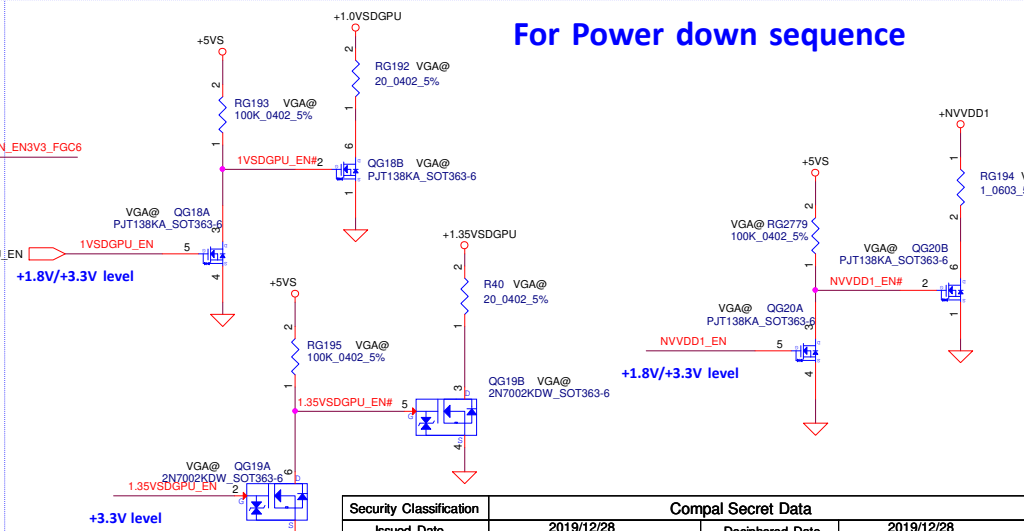


1.8VSDGPU_MAIN_EN_FGC6

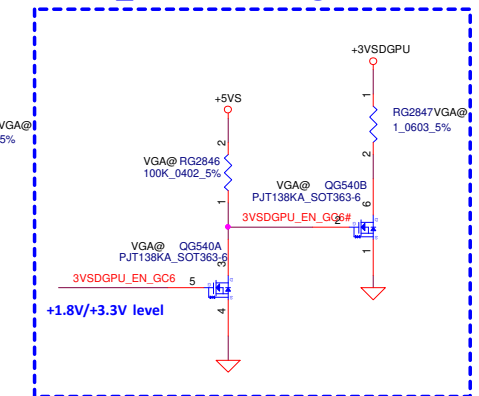


EH50F change to AOZ1334DI-02

For Power down sequence

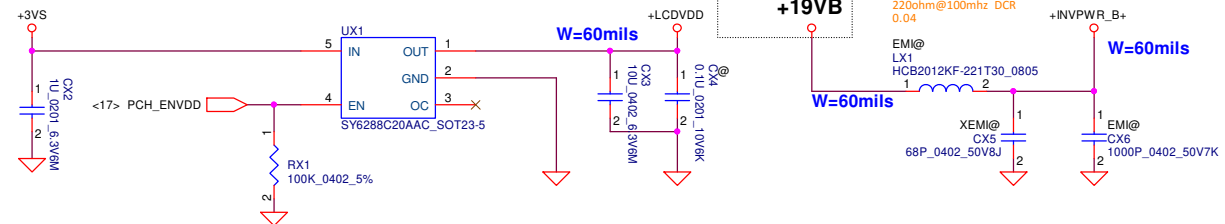


+3VSD_GPU discharge if need

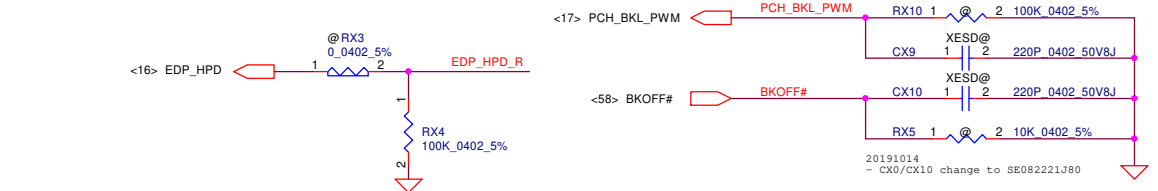


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				N18E-GPU Power control	
				Size	Document Number
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				Date:	Wednesday, February 26, 2020
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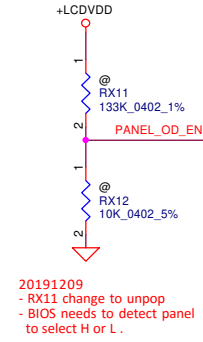
LCD POWER CIRCUIT



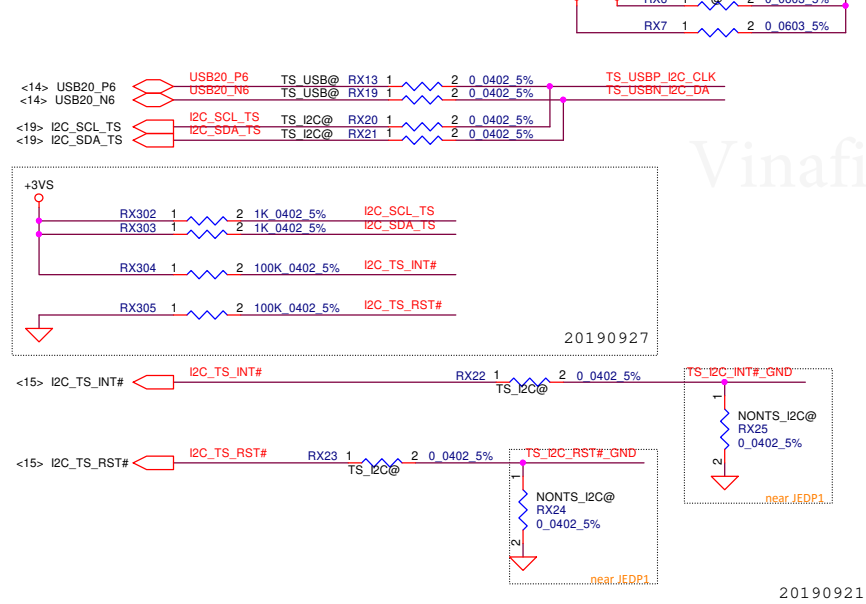
LCD enable signal



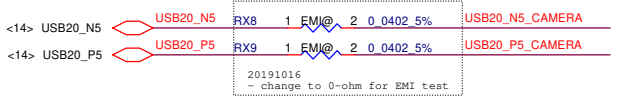
Panel OD



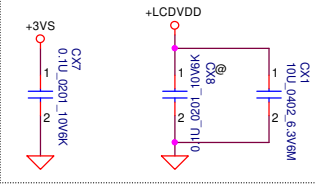
USB/I2C Touch Screen Co-Lay



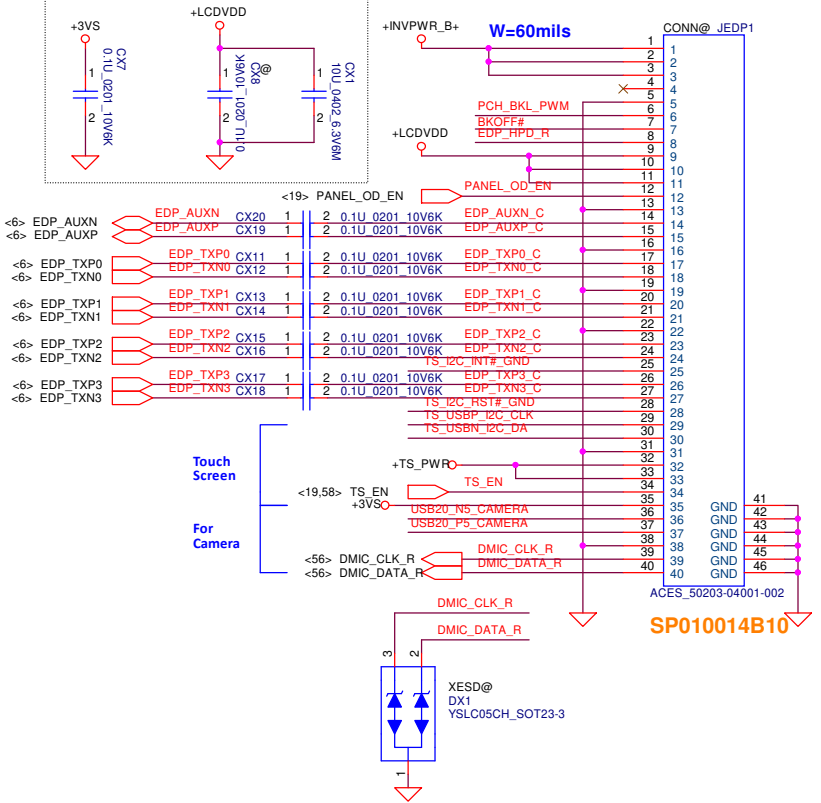
CAMERA



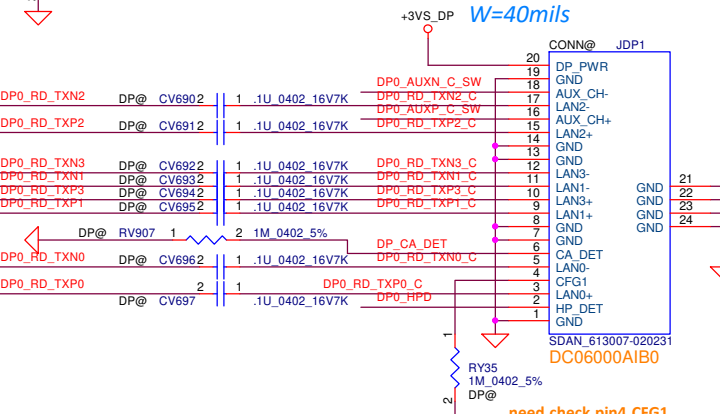
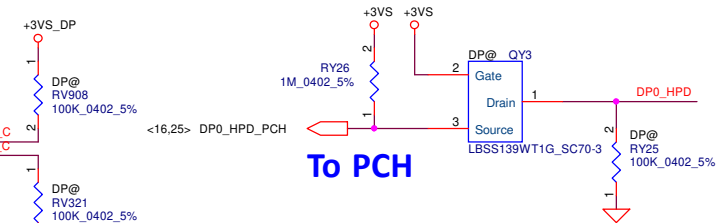
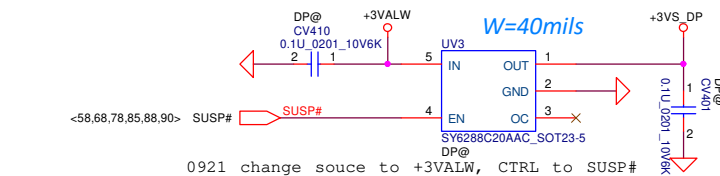
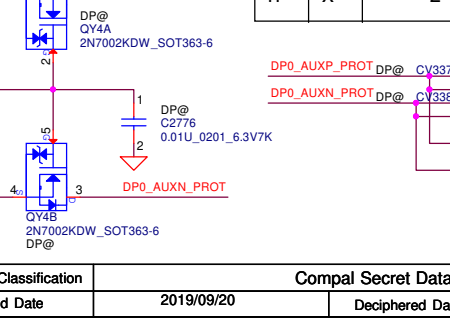
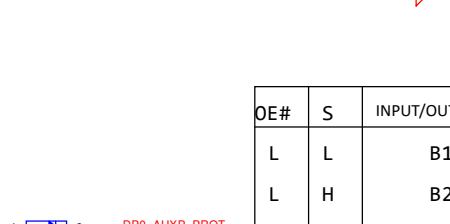
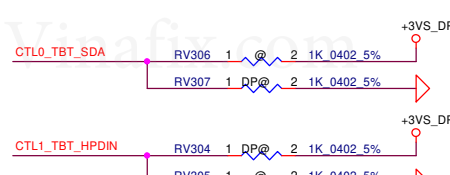
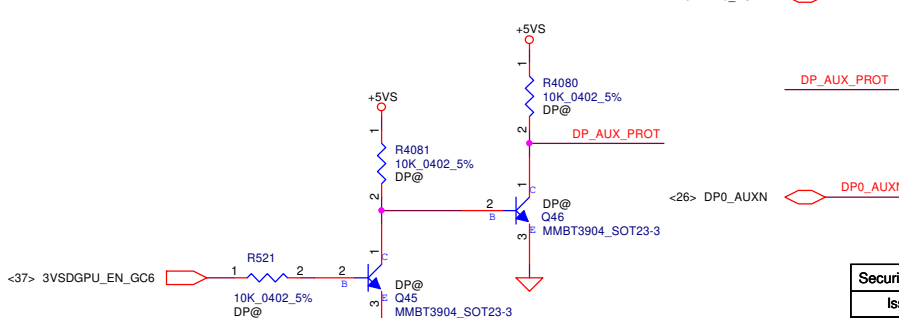
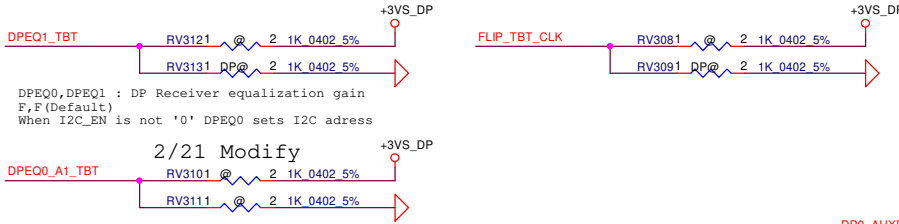
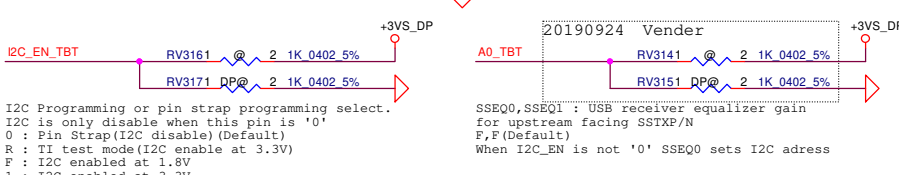
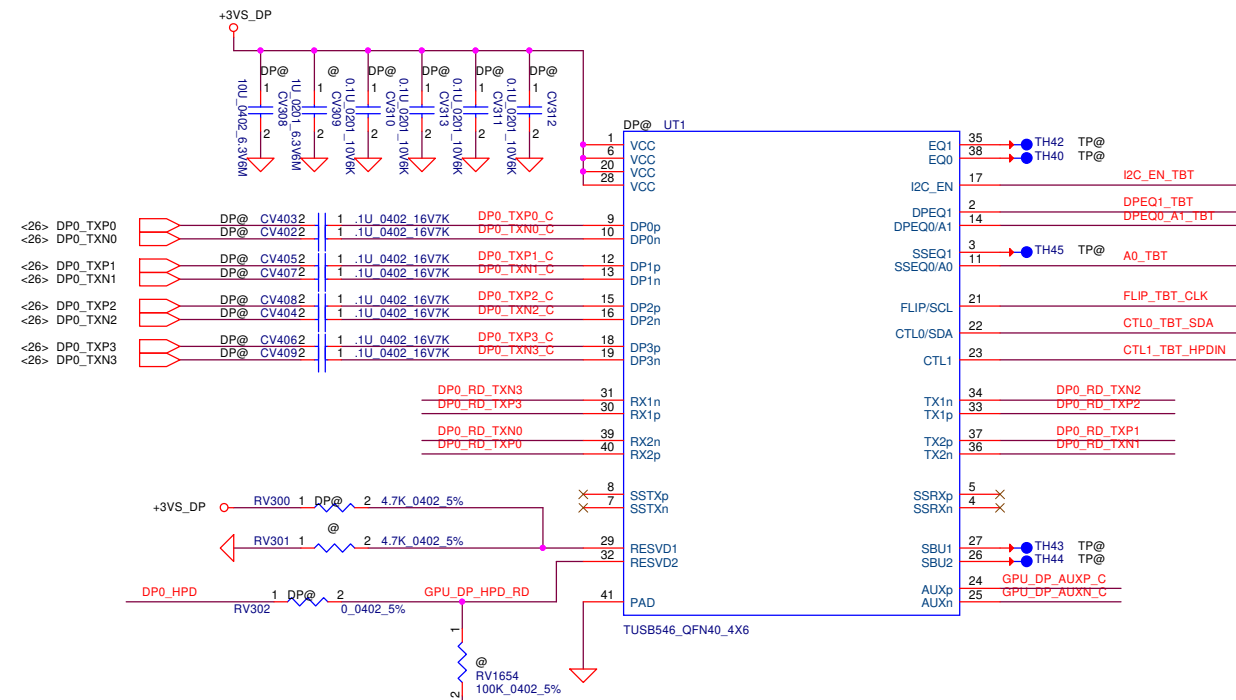
Place closed to JEDP1



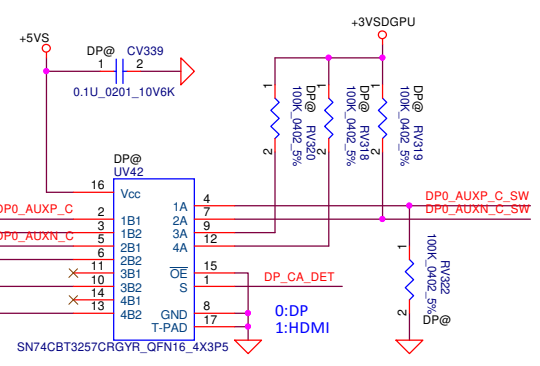
LED PANEL Conn.



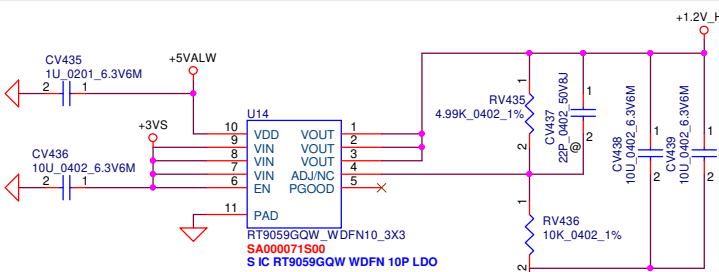
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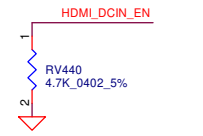
OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC



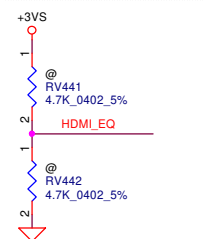
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Issued Date		2019/09/20		Deciphered Date		2020/09/20		Title			
								DP CONN (TUSB546)			
Size		Document Number		Date		Wednesday, February 26, 2020		Sheet		39 of 112	
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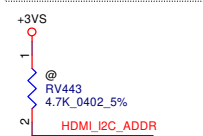
DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default, AC coupling input



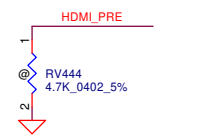
Receiver equalization setting (Internal 150K PD)
(*) L: programmable EQ for channel loss up to 5.3dB
() H: programmable EQ for channel loss up to 10dB
() M: programmable EQ for channel loss up to 14dB



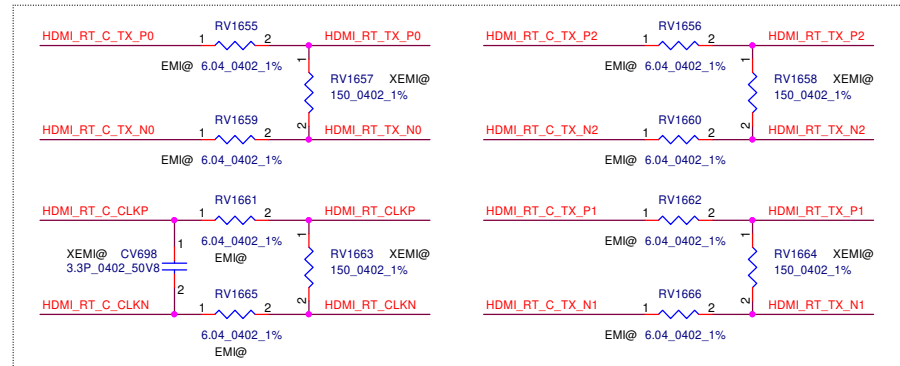
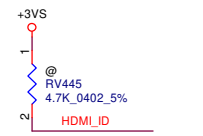
I2C Slave Address selection; Internal pull down; 3.3V I/O
L: Default, Slave address 0x10-0x2F
H: Alternative slave address 0x90-0x9F, 0xD0-0xDF.



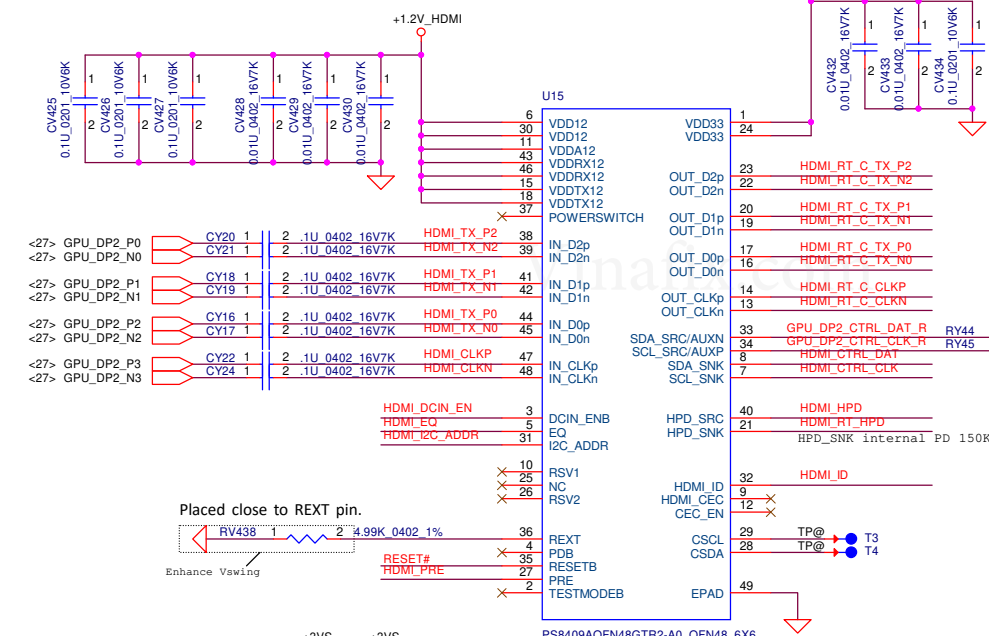
Output pre-emphasis setting; Internal pull-up 3.3V I/O
L: Pre-emphasis +2.5dB
H: Default, No Pre-emphasis



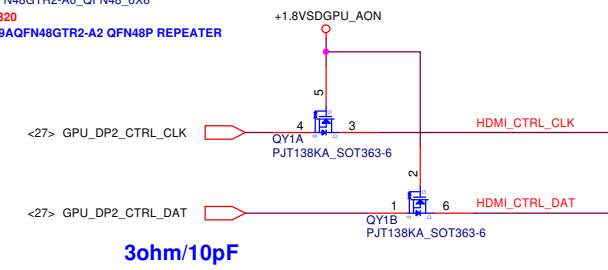
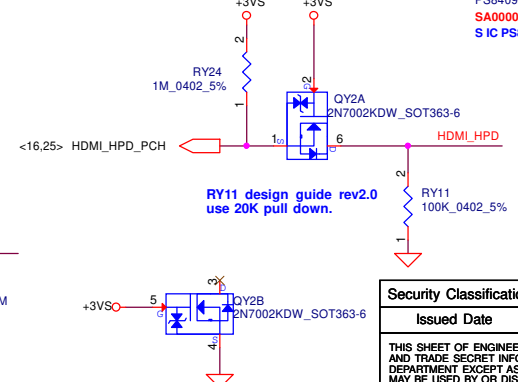
HDMI ID enable; Internal pull down; 3.3V I/O
L: Default, HDMI ID enable
H: HDMI ID disable



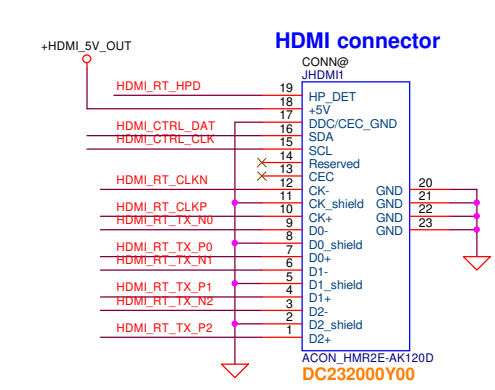
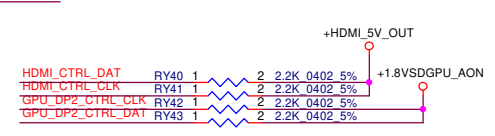
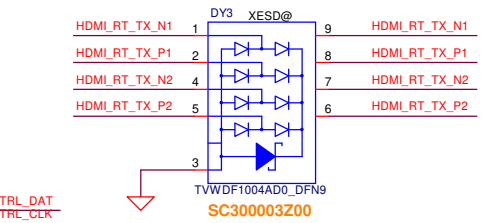
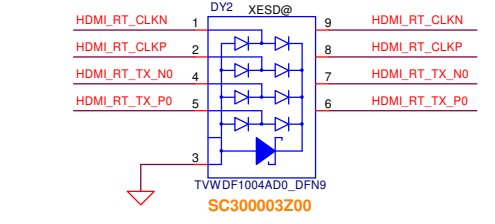
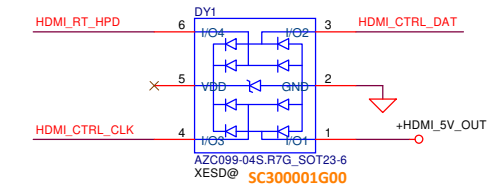
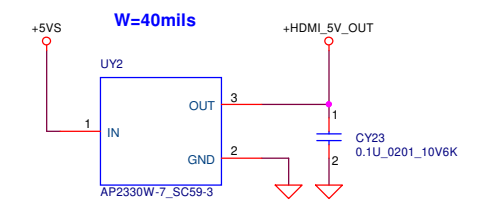
20191015, EMI



Placed close to REXT pin.
Enhance Vswing



3ohm/10pF



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VRAM

N18E-G0

MICRON 1.35V

SAMSUNG 1.35V

GPU



N18EG0@
SA0000CK430
S IC D6 256M32 MT61K256M32JE-14-A ABO



N18EG1B@
SA0000DEX10
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO



N18EG1R@
SA0000D4N40
S IC D6 256M32 K4Z80325BC-HC14 FBGA ABO !

X76



X76L05@
ALT. GROUP PARTS MIC VRAM 6G FH51M
X76869BOL05



X76L06@
ALT. GROUP PARTS SAM VRAM 6G FH51M
X76869BOL06



X76L07@
ALT. GROUP PARTS MIC VRAM 8G FH51M
X76869BOL07



X76L08@
ALT. GROUP PARTS SAM VRAM 8G FH51M
X76869BOL08



X76L11@
ALT. GROUP PARTS MIC 1.35V VRAM 6G FH51M
X76869BOL11



X76L12@
ALT. GROUP PARTS SAM 1.35V VRAM 6G FH51M
X76869BOL12

OVRM



X76L09@
ALT. GROUP PARTS OVRM EG0G1G1R ON FH51M
X76869BOL09



X76L10@
ALT. GROUP PARTS OVRM EG0G1G1R UPI FH51M
X76869BOL10

N18E-G1B

MICRON 1.2V

SAMSUNG 1.2V

Vinafix.com

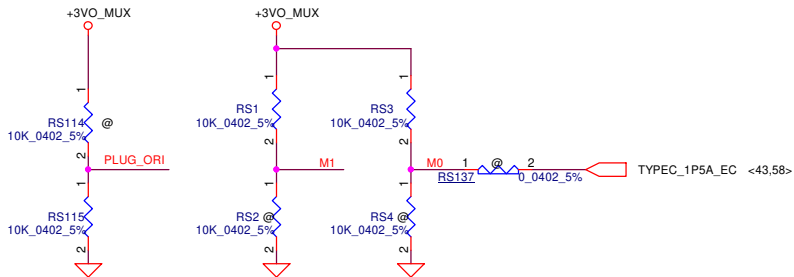
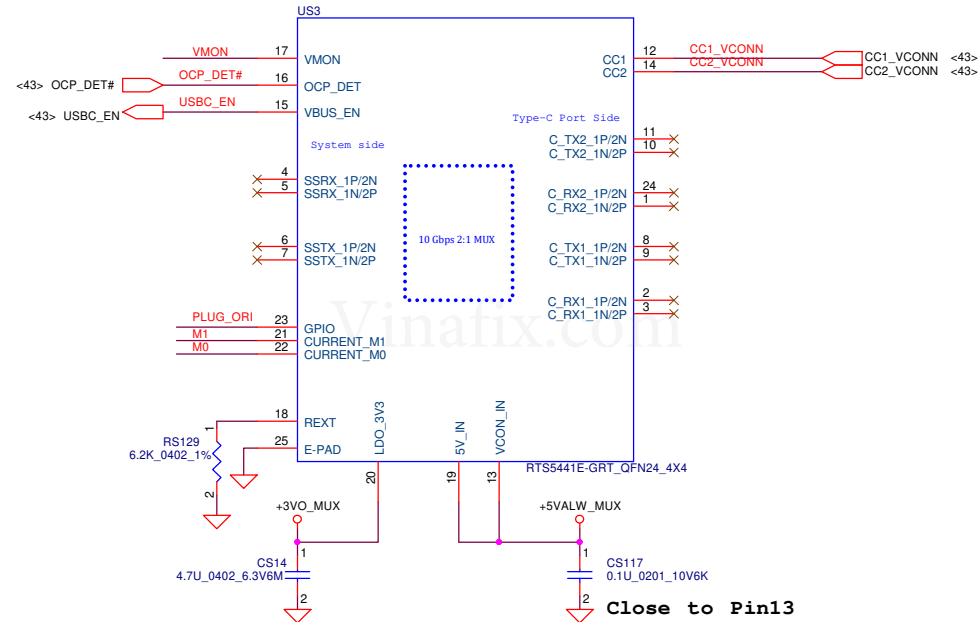
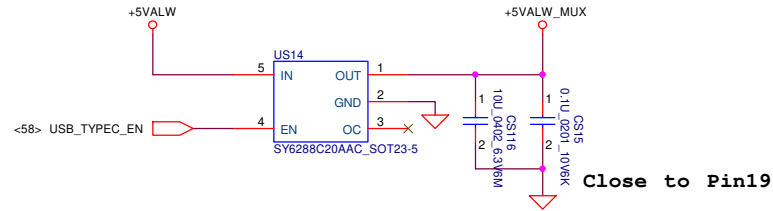
N18E-G1R

MICRON 1.2V

SAMSUNG 1.2V

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20191014
- Change to "with no Dual Role support"
- 5441E only uses the function of CC & Power SW



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

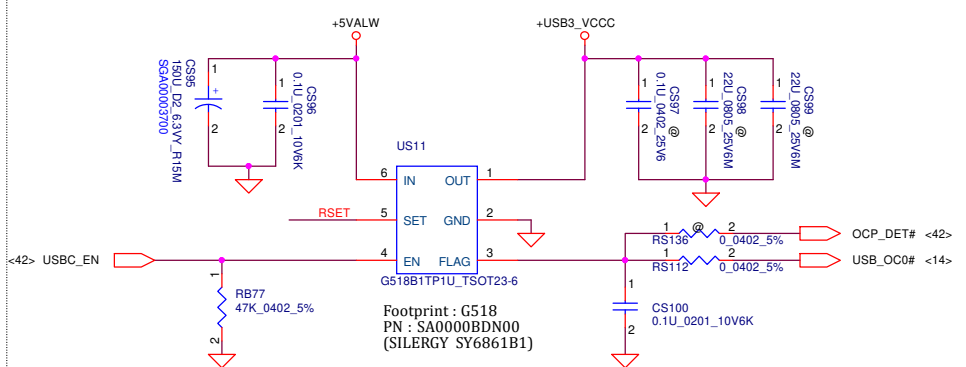
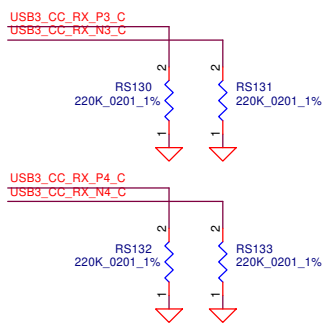
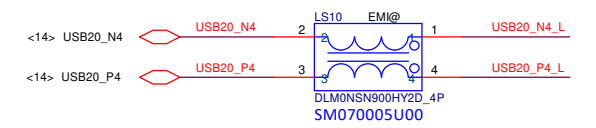
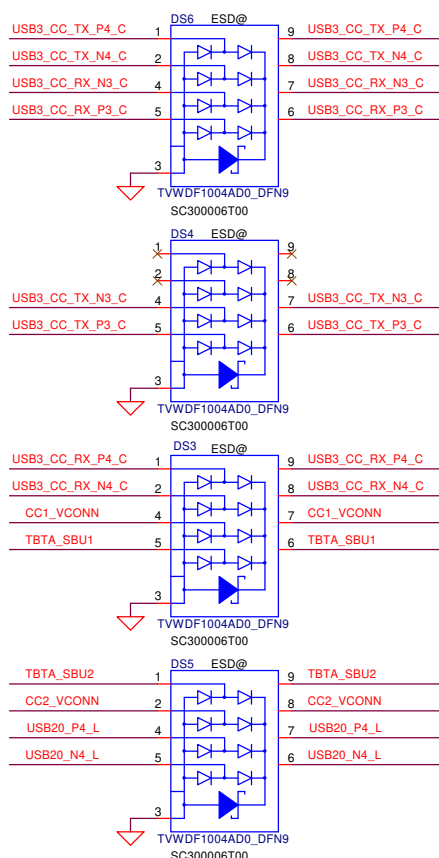
confirm realtek hand-shake			
RTS5441 M0 truth table by 2018 BIOS spec			
TYPE1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

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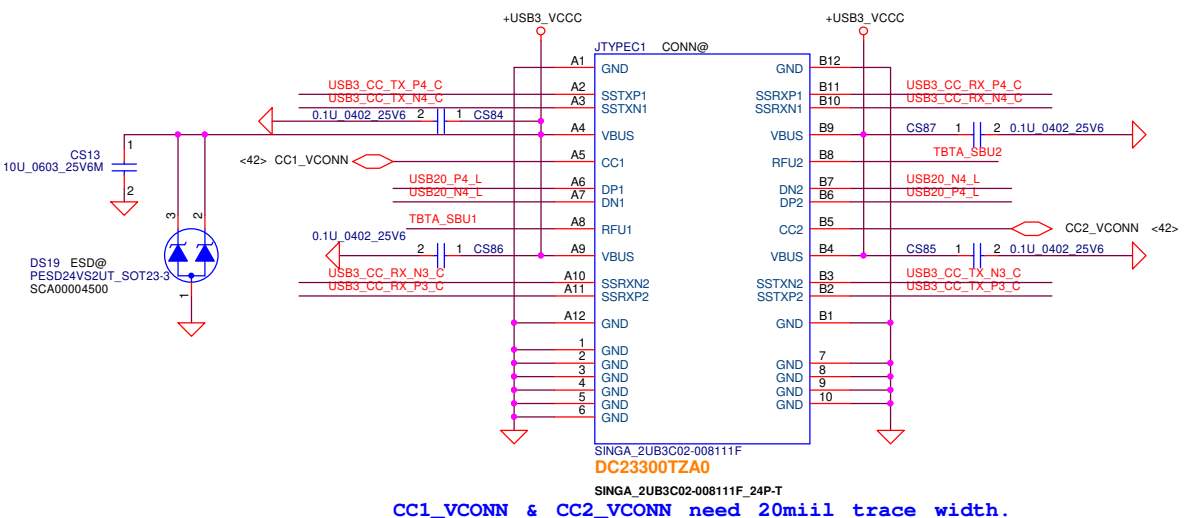
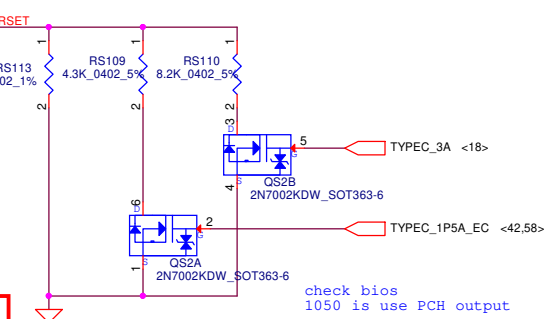
20191014
- Change to "with no Dual Role support"
- CS112/113/114/115 change to 0.33U

20191016
- USB3 Port5 change to Port3

20191015 - Pin SWAP for layout
20191016 For ESD request - Gen2 Solution SC300006T00



G518 MOS Current Limit					
GPP_B1 TYPE_C_1P5A	GPP_B4 TYPE_C_3A	RSET(kΩ)	MODE	limit point	
L	L	6.2	0.9A	1.09A	
L	H	3.53	1.5A	1.92A	
H	L	2.54	2A	2.67A	
*H	H	1.94	3A	3.5A	



CC1_VCONN & CC2_VCONN need 20mil trace width.

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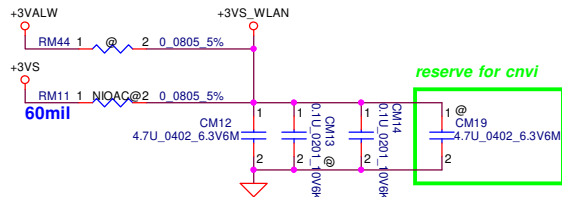
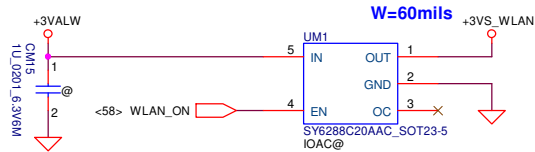
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20190918
LAN more to IO/B

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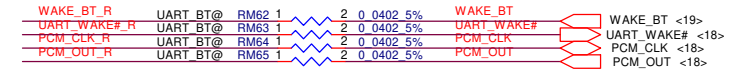
Wireless LAN



20191211 [FH51M CNVi review]
> RM69 change to 71.5k & CNVi@
> RM70 set CNVi@
> RH22 change to 20K
> RM36/RM37/RM67/RM68 change to 22 ohm
> RM16 recommend to 4.7K (no action)
> RH199 recommend to pop (no action)
> RM45 recommend to 10K (no action)
> WL_OFF# recommend to PU 10K (no action)

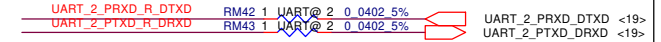
20191209 [FH51M CNVi review]
Pin10 - RM41 Close to PCH
Pin14 - CLKREQ_CNVi# PD RM69(71.5K) (Reserve)
Pin20 - UART_WAKE PU RM70(4.7K) (Reserve)
Pin22 - RM36@M.2 / RH181@PCH
Pin32 - RM37@PCH / RH22@M.2
Pin34 - RM67@M.2 / RH182@PCH
Pin36 - RM68@PCH / RH15@M.2

UART BT



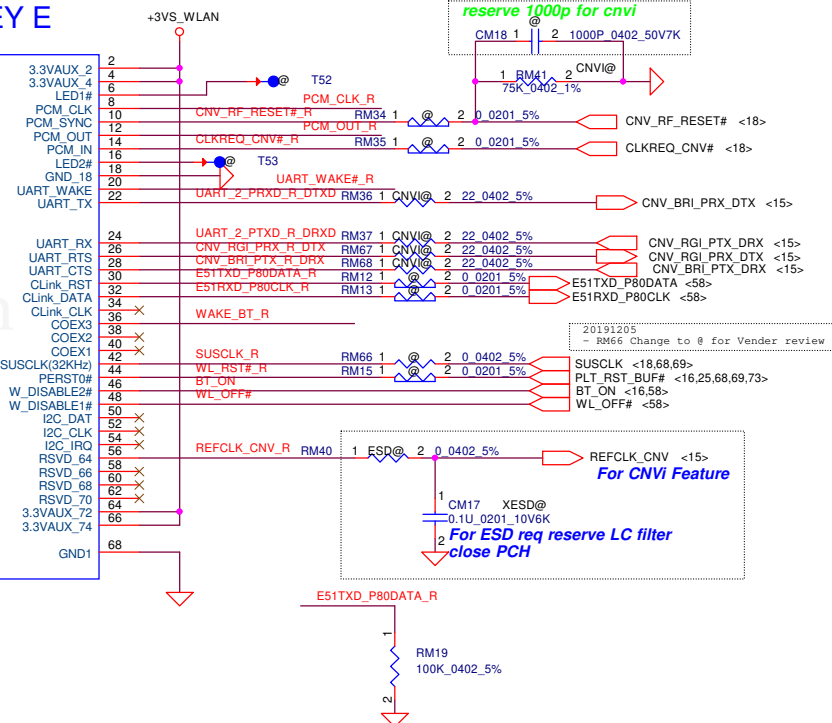
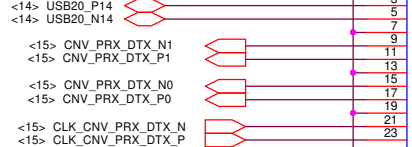
20191007
- Add RM62/63/64/65

Co-layout with CNVi for SW debug



KEY E

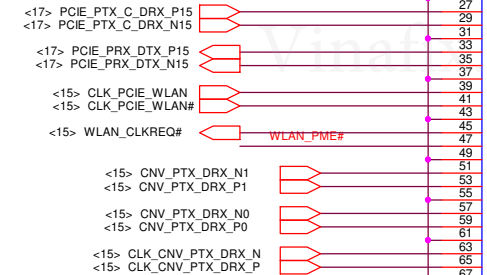
(For BT)



NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLK_N1	73
70	UM_Power_SRC(GPIO/PEWake#	RESERVED/REFCLK_P1	71
68	UM_Power_SINK(CLKREQ#	GND	69
66	Reserved/PERn1	Reserved/PERn1	67
64	Reserved	Reserved/PERn1	65
62	ALERT# (IO/Q3.3)	Reserved/PETn1	61
60	OC CLK (IO/Q3.3)	Reserved/PETn1	59
58	OC DATA (IO/Q3.3)	Reserved/PETn1	57
56	WL_DISABLE#1 (IO/Q3.3V)	PEWake# (IO/Q3.3V)	55
54	Reserved/WL_DISABLE#2 (IO/Q3.3V)	CLKREQ# (IO/Q3.3V)	53
52	PERST# (IO/Q3.3V)	GND	51
50	SUSCLK(32KHz) (IO/Q3.3V)	REFCLK_N0	49
48	COEX1 (IO/Q1.8V)	REFCLK_P0	47
46	COEX2 (IO/Q1.8V)	GND	45
44	COEX3 (IO/Q1.8V)	PERn0	43
42	VENDOR DEFINED	PERn0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART RTS (IO/Q1.8V)	PETn0	35
34	UART CTS (IO/Q1.8V)	GND	33
32	UART Tx (IO/Q1.8V)	GND	31

(link to PICE Port 3)
PCIE X1
(From PCH CLKOUT2)
PCIE CLK



reserve for BT_ON OD pull high (1.0)



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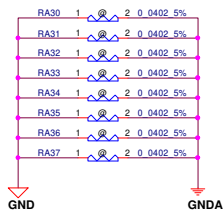
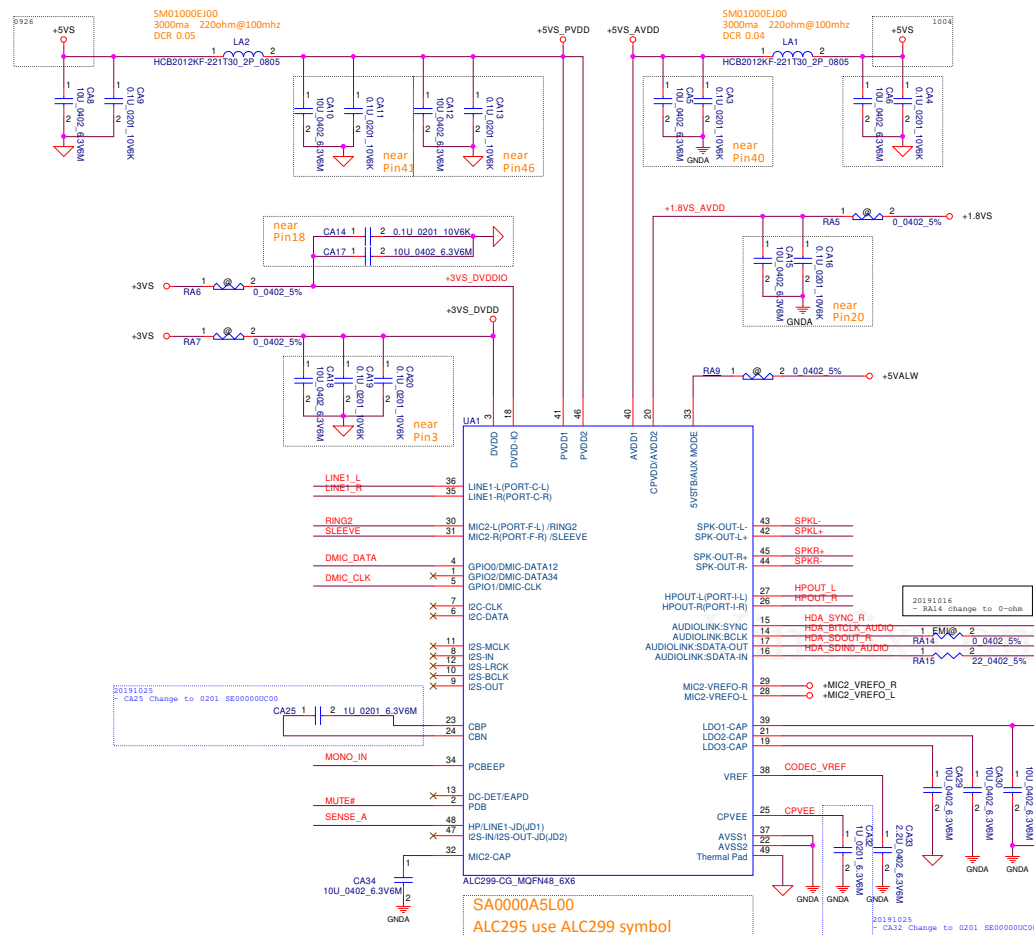
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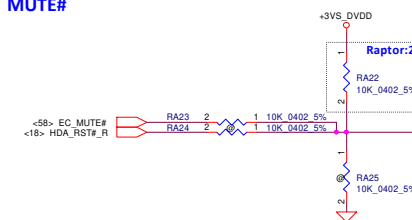
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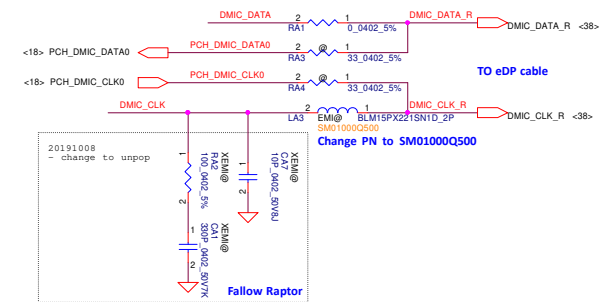
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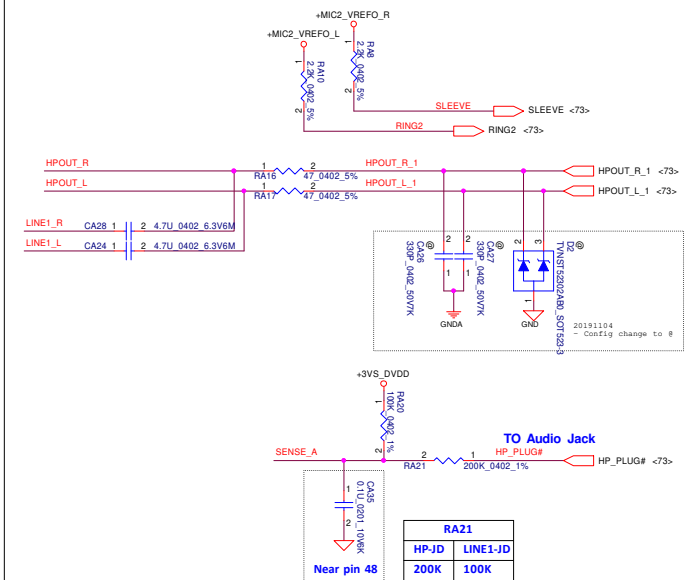
MUTE#



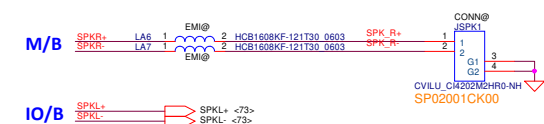
Digital MIC



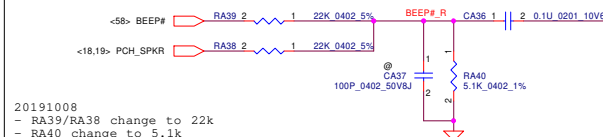
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Speaker



BEEP

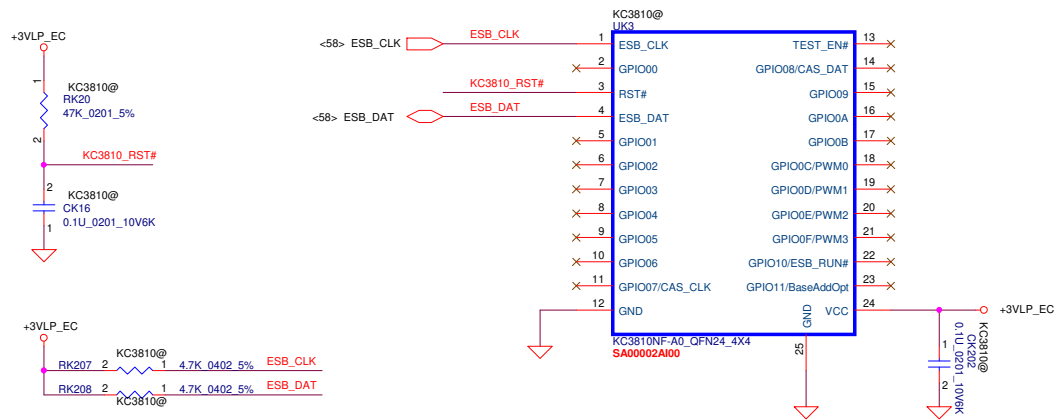


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*NMI_DBG#; is a debug pin for EC to
infrom BIOS after press hot key.
OMEN New ESB CLK&DAT for Extend I/O

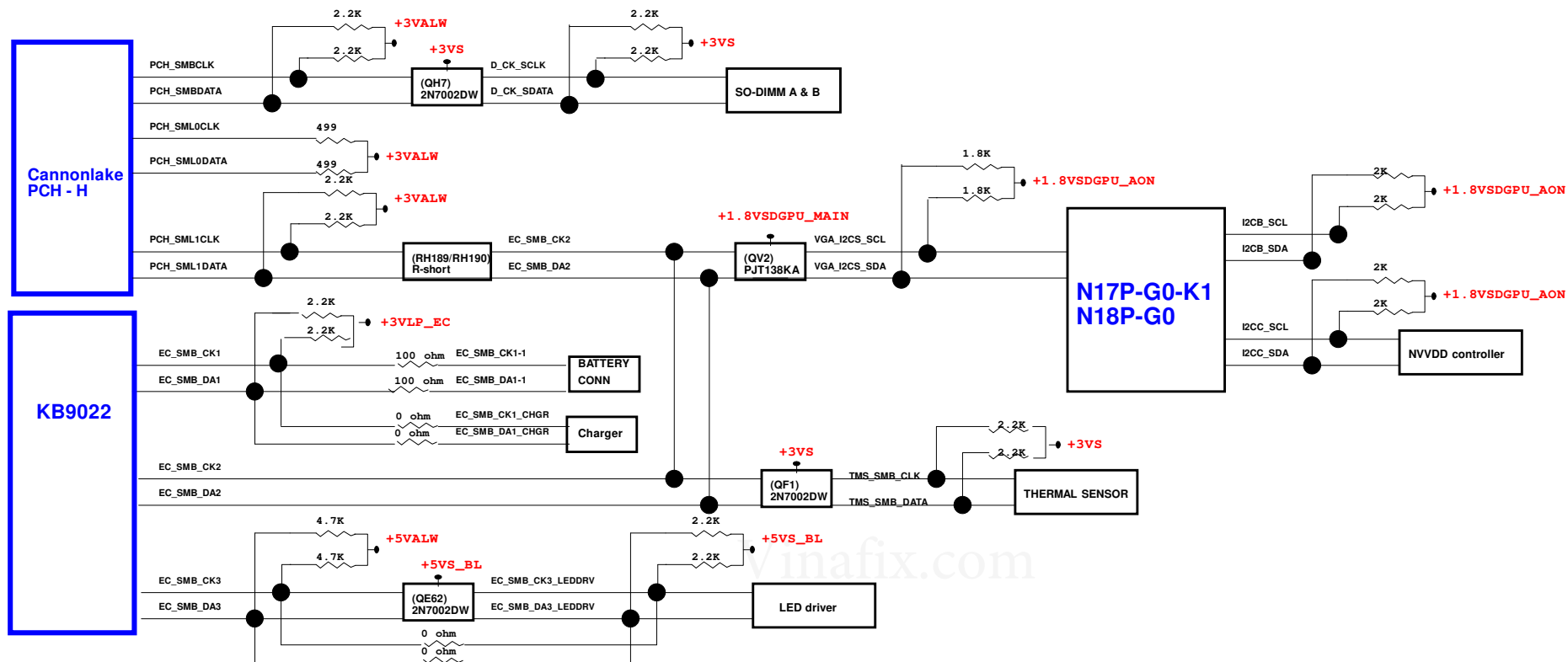


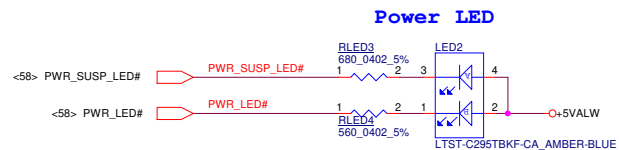
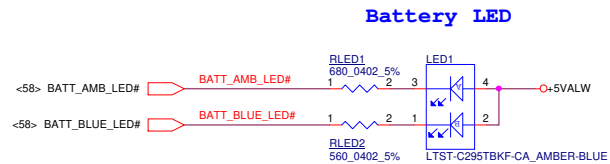
Vinafix.com

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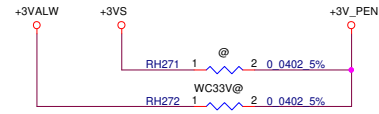




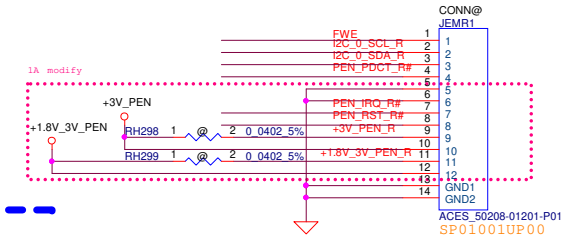
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				Size	Document Number
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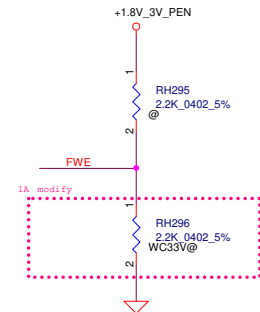
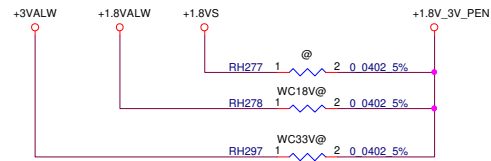
3V_PEN



EMR

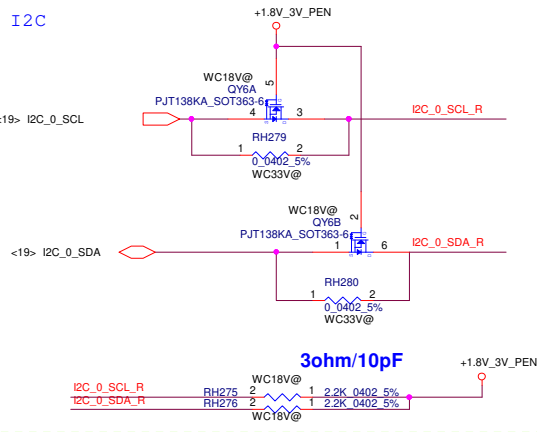


1.8V_PEN

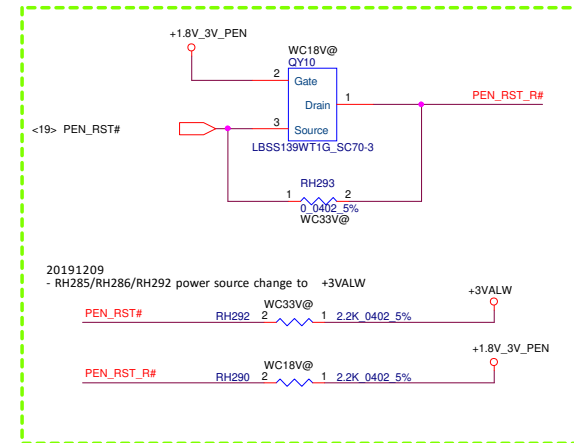
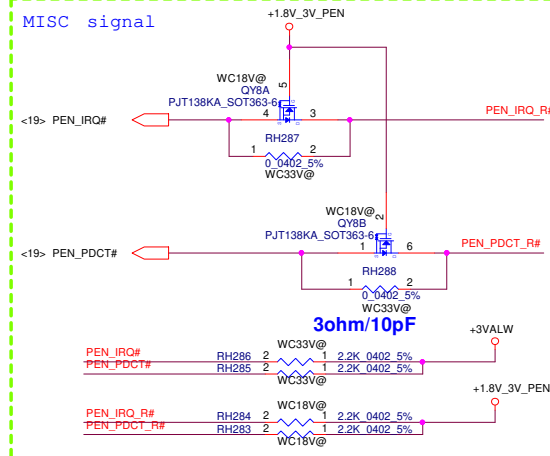


20191008
- QY6/QY8 change to SB000016K00
Default use 0ohm(WC33V@)

I2C



MISC signal

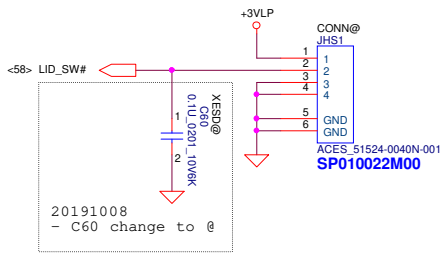


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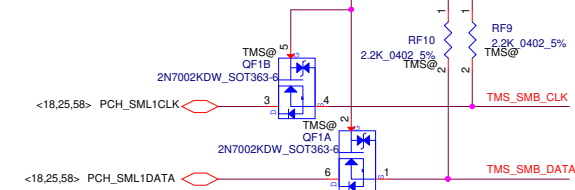
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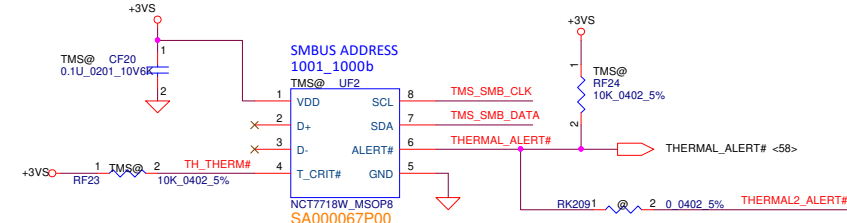
To Hall sensor/B



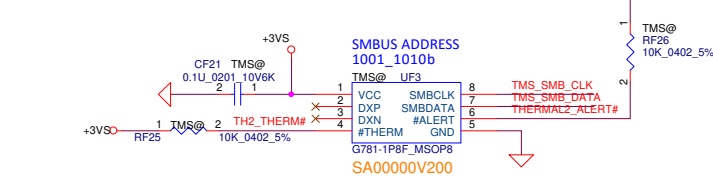
THERMAL SENSOR



Close to SO-DIMM

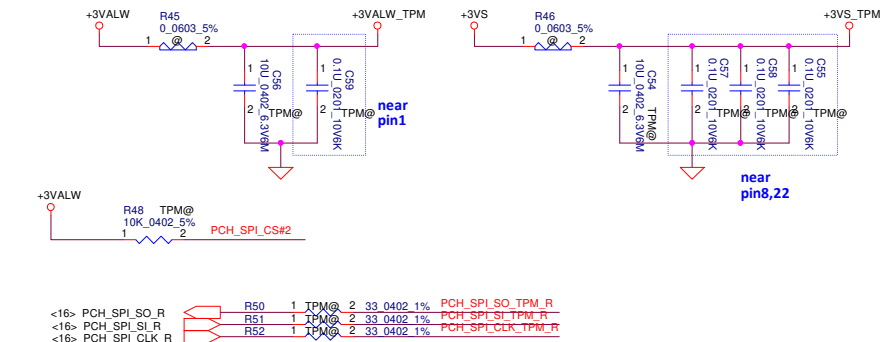


Close to Thermal SKIN

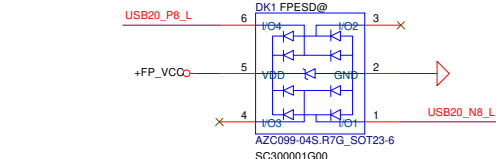
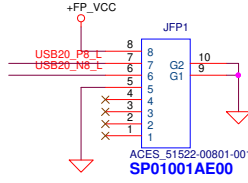
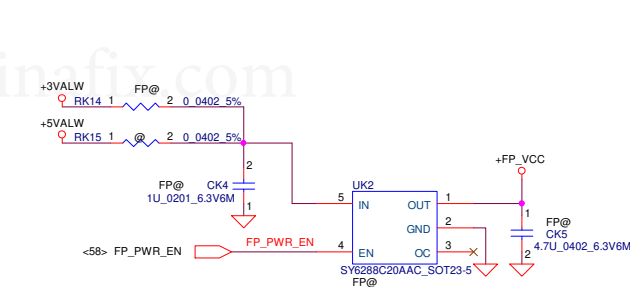


Thermal resister on PWR side, 10/16

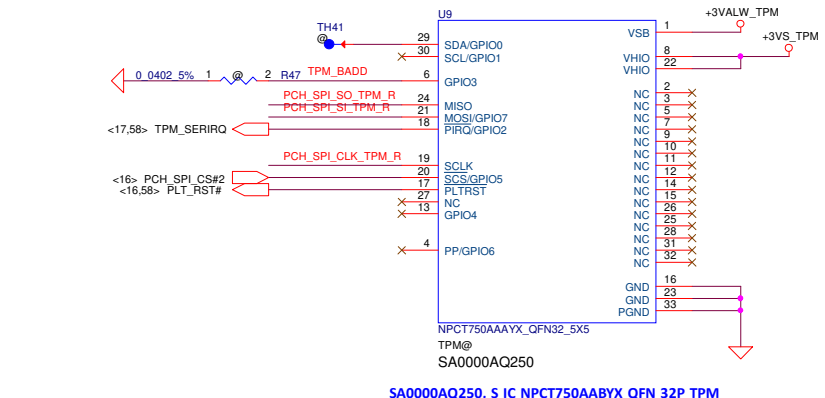
TPM



Finger Print

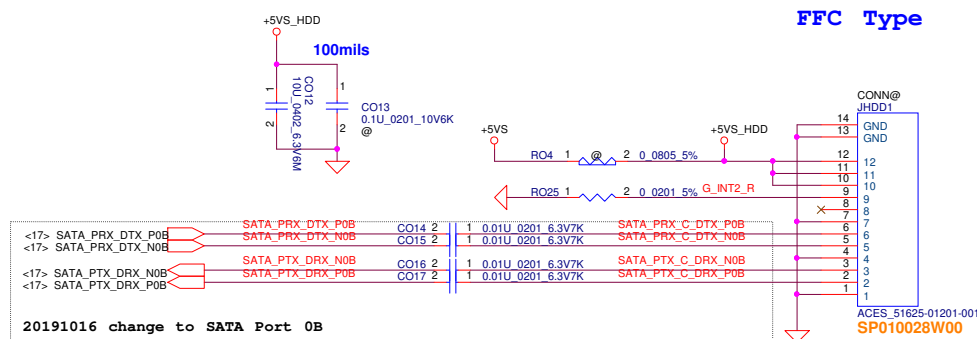


PIN	ETU801	FA6780-2202
1	+FP_VCC (5V)	+FP_3.3_FP
2	USBP	USBP
3	USBN	USBN
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC



SA0000AQ250, S IC NPCT750AABYX QFN 32P TPM

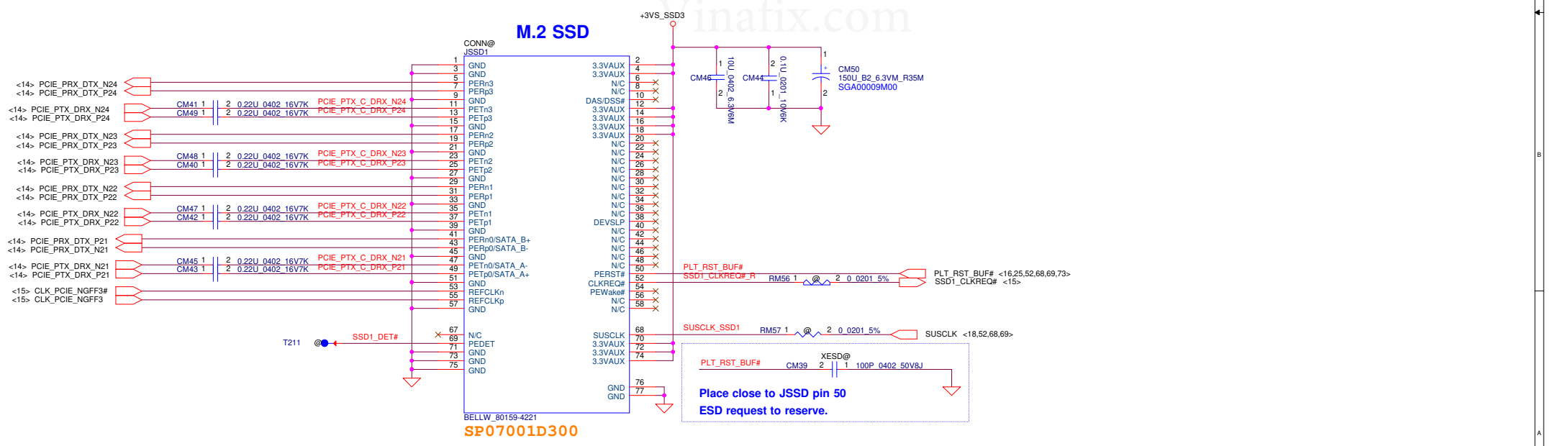
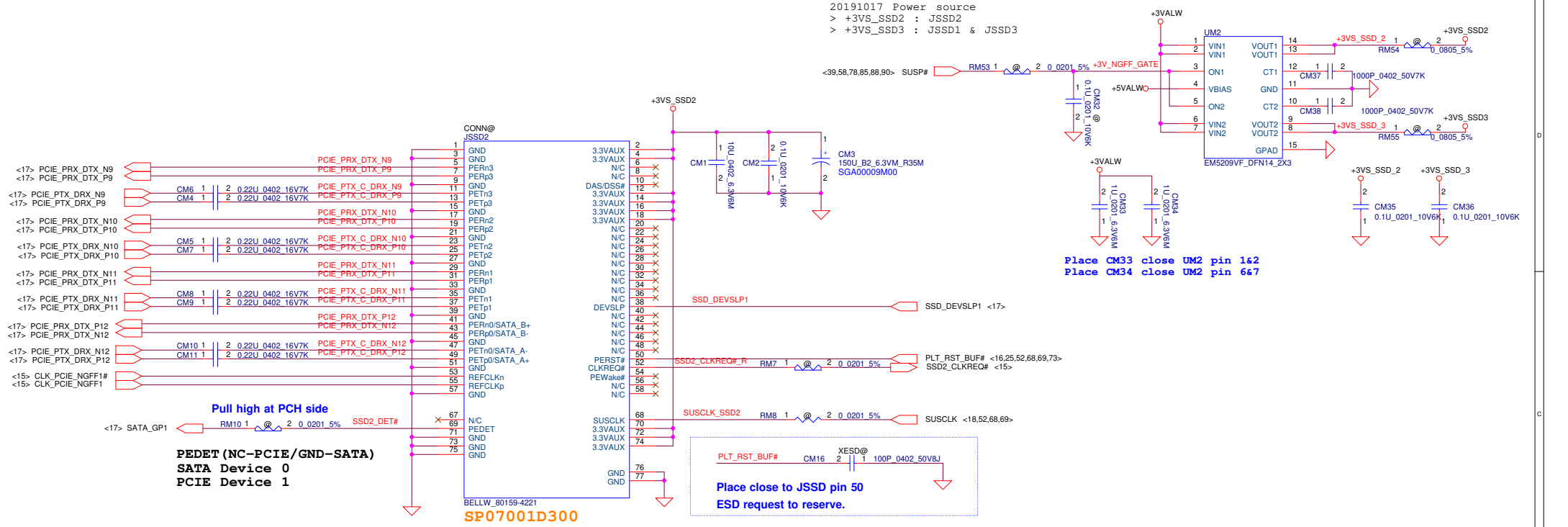
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Title		Sensors/FP/TPM	
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20190918

Remove HDD Re-driver

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										HDD/ Re-Driver/ G-sensor	
										Size Document Number	
										FH51M M/B LA-J871P	
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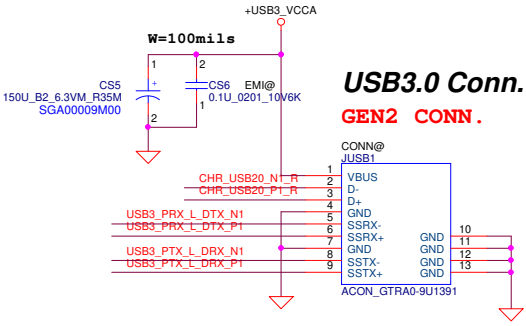
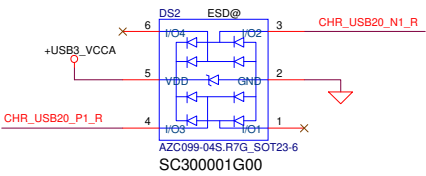
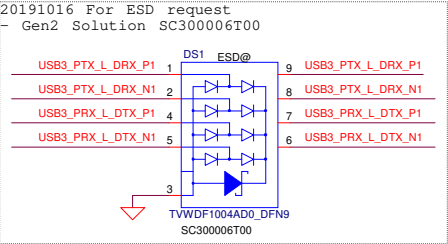
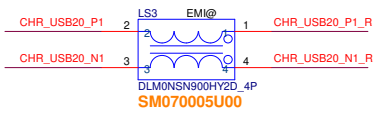
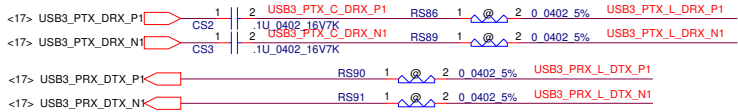


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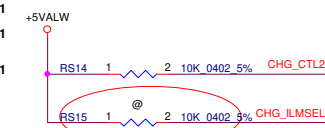
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USB3.0



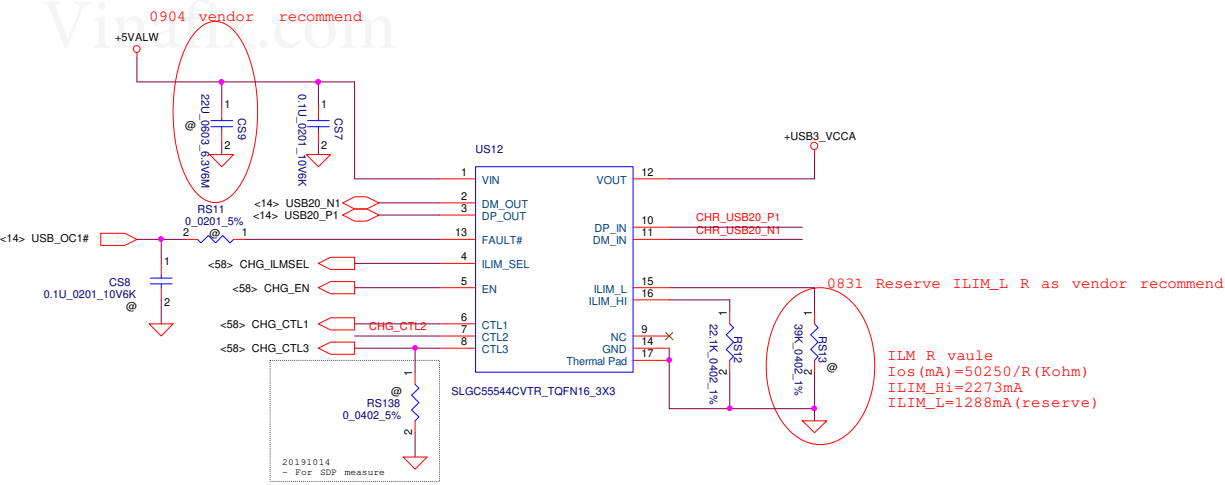
USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	1	0	1	SDP1-OFF	ILIM_H	Port power off	
0	1	0	1	SDP1	ILIM_H	Data Lines Connected	
0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected	
1	1	1	1	CDP	ILIM_H	Data Lines Connected	

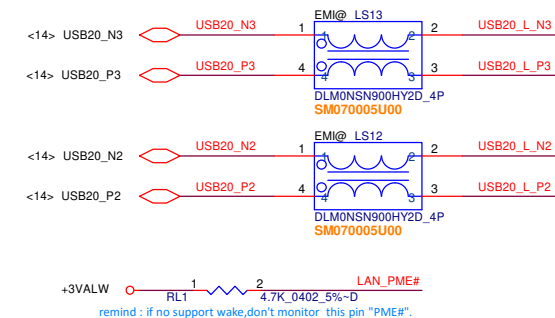


20190918

USB3 Port3 move to IO/B

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IO/B CONN



1211
- IO_B change pin define

20191008
- LAN PCIE&CLK Remove AC Cap > Vender confirm
(CL136/137/138/139)

20191016
- Change to Port5

<17> USB3_PTX_DRX_P5
<17> USB3_PTX_DRX_N5
<17> USB3_PRX_DTX_P5
<17> USB3_PRX_DTX_N5

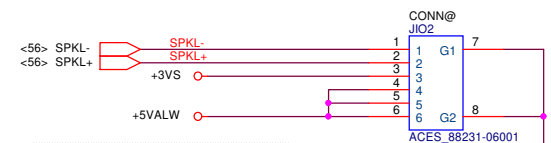
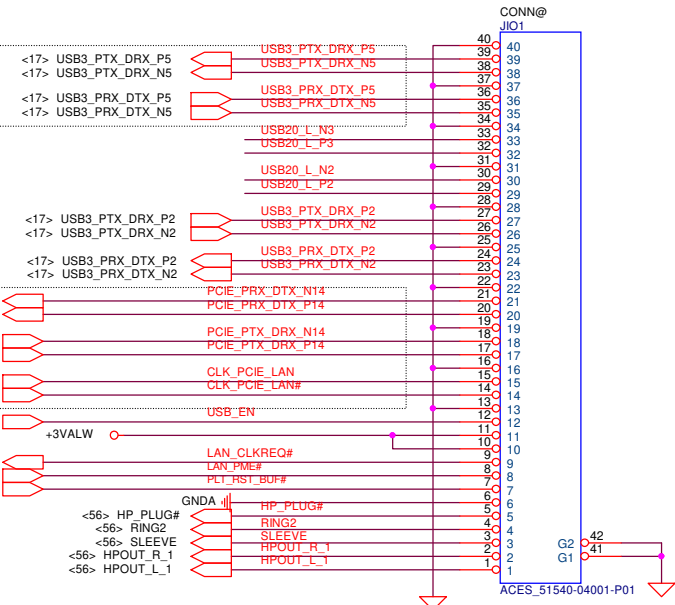
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<15> CLK_PCIE_LAN
<15> CLK_PCIE_LAN#

<58> USB_EN

<15> LAN_CLKREQ#
<16,58> EC_PME#
<16,25,52,68,69> PLT_RST_BUF#

<56> HP_PLUG#
<56> RING2
<56> SLEEVE
<56> HPOUT_R_1
<56> HPOUT_L_1



20191023
- Add +3VS

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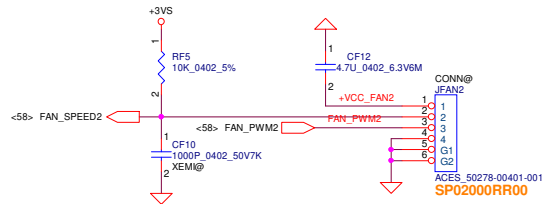
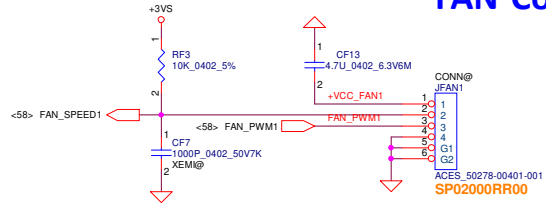
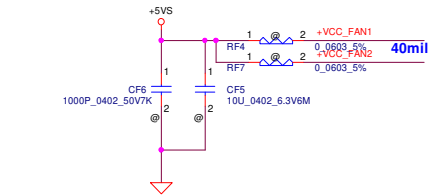
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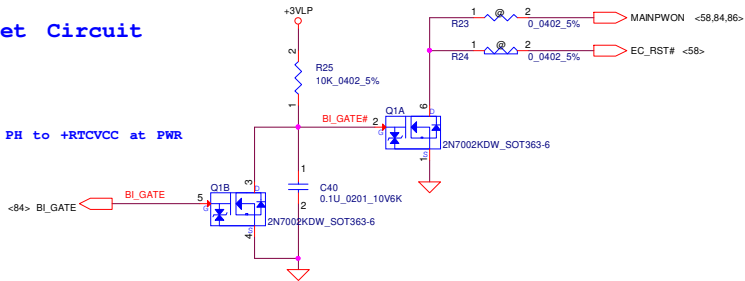
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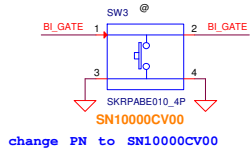


Reset Circuit

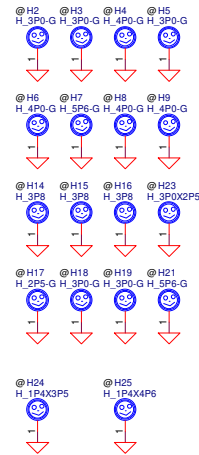
BI_GATE PH to +RTCVCC at PWR side



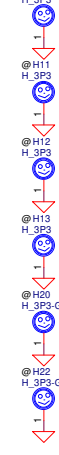
Reset Button



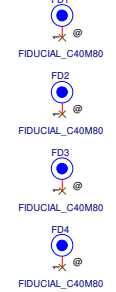
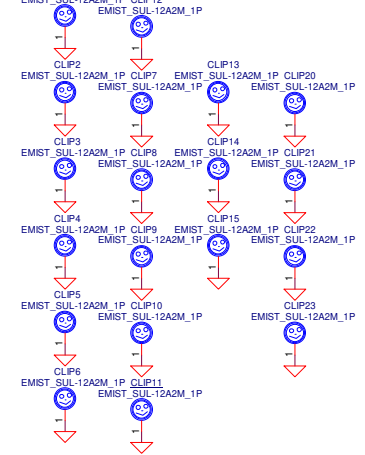
Screw Hole



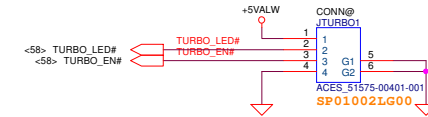
Stand OFF



Clips



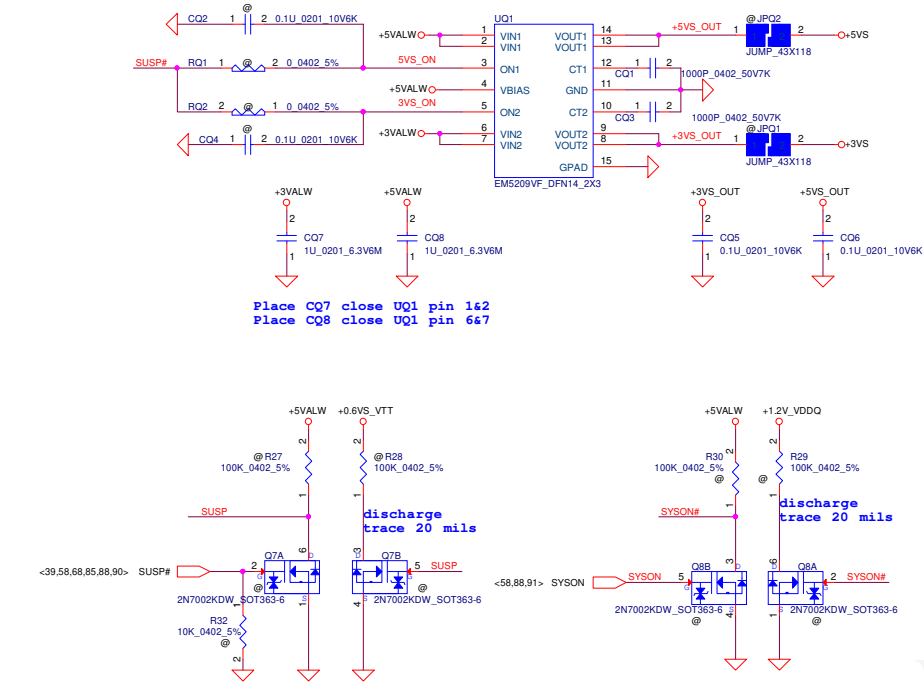
Turbo Key



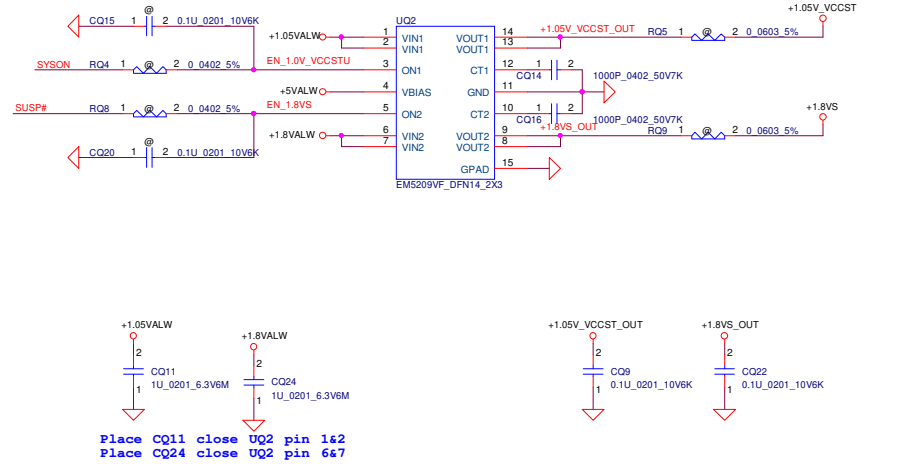
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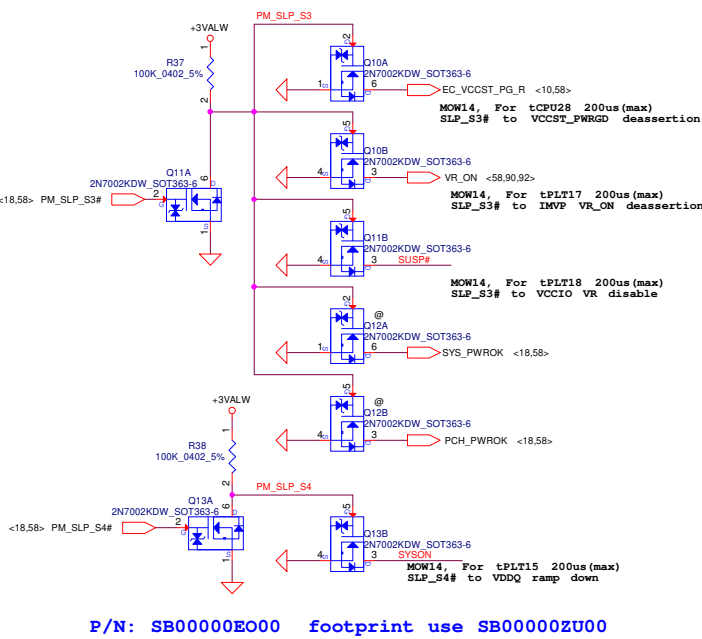
System DC interface



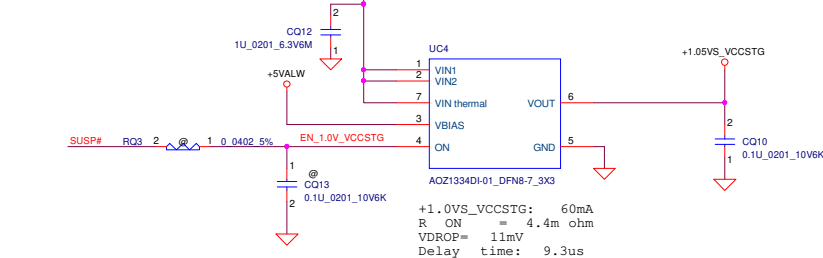
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



For Power ON/Off Sequence



+1.05VALW TO +1.05VS_VCCSTG



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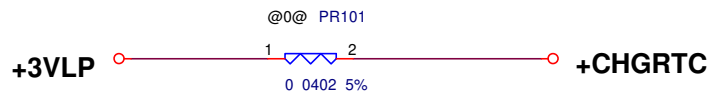
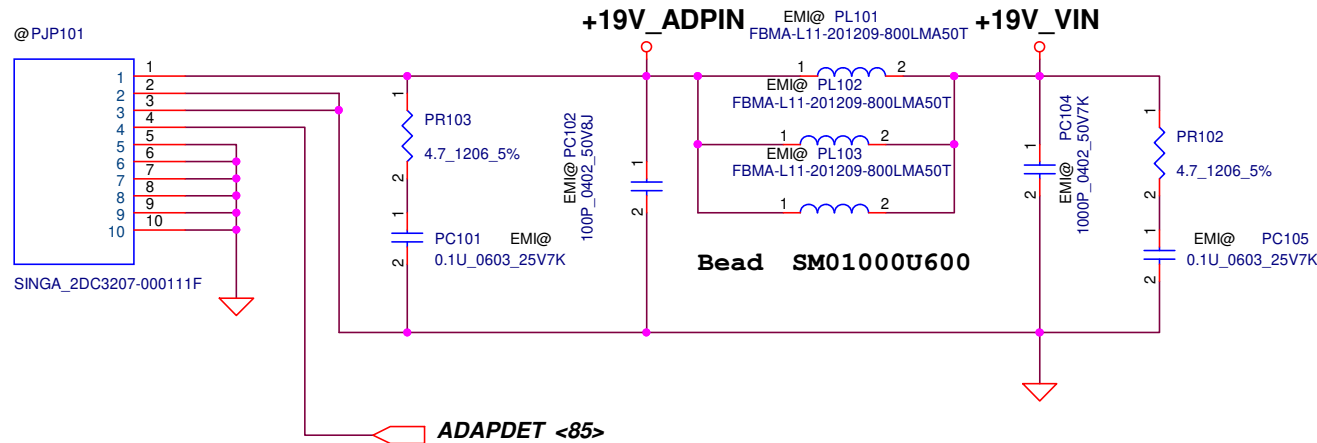
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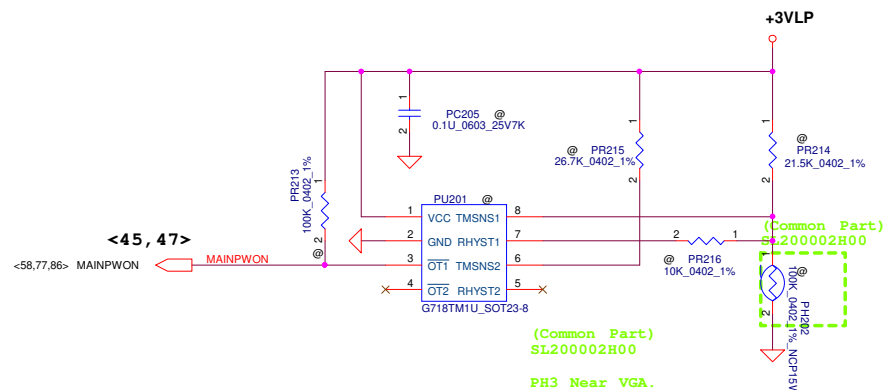
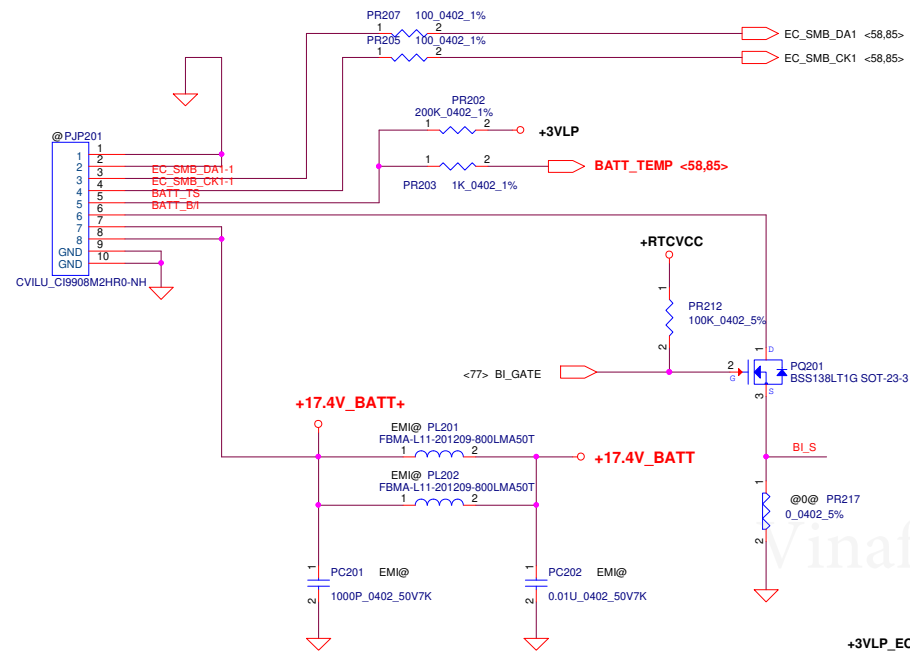
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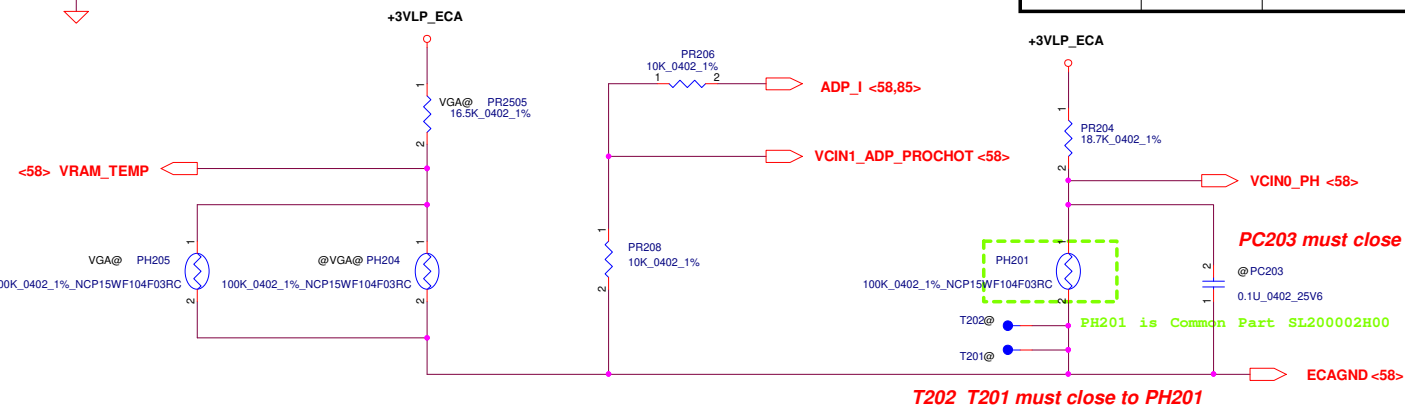
Battery Bot Side

- PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+

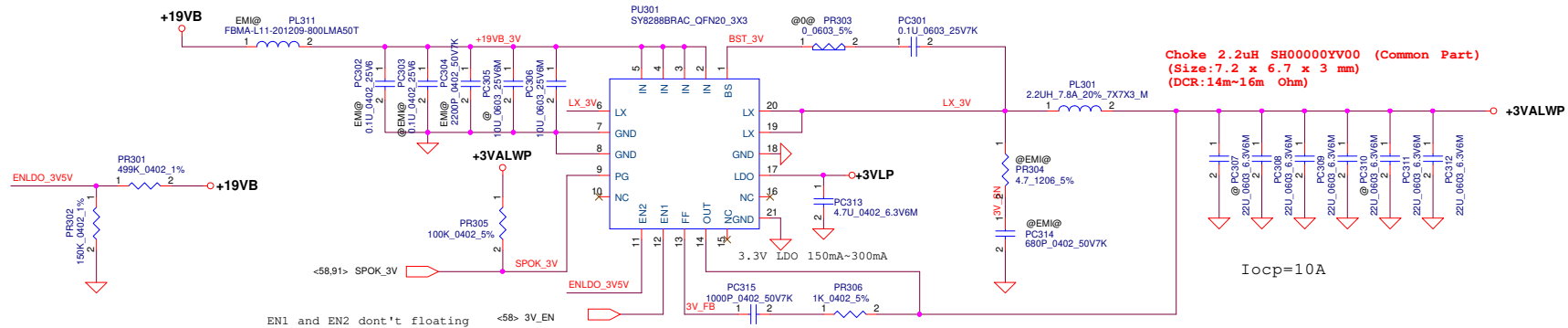


When PR204=18.7K

For	KB9022	Active	Recovery
OTP			
VCIN0_PH (V)	89'C, 1V	56'C, 2V	
PH202 (ohm)	8.0524K	26.11K	

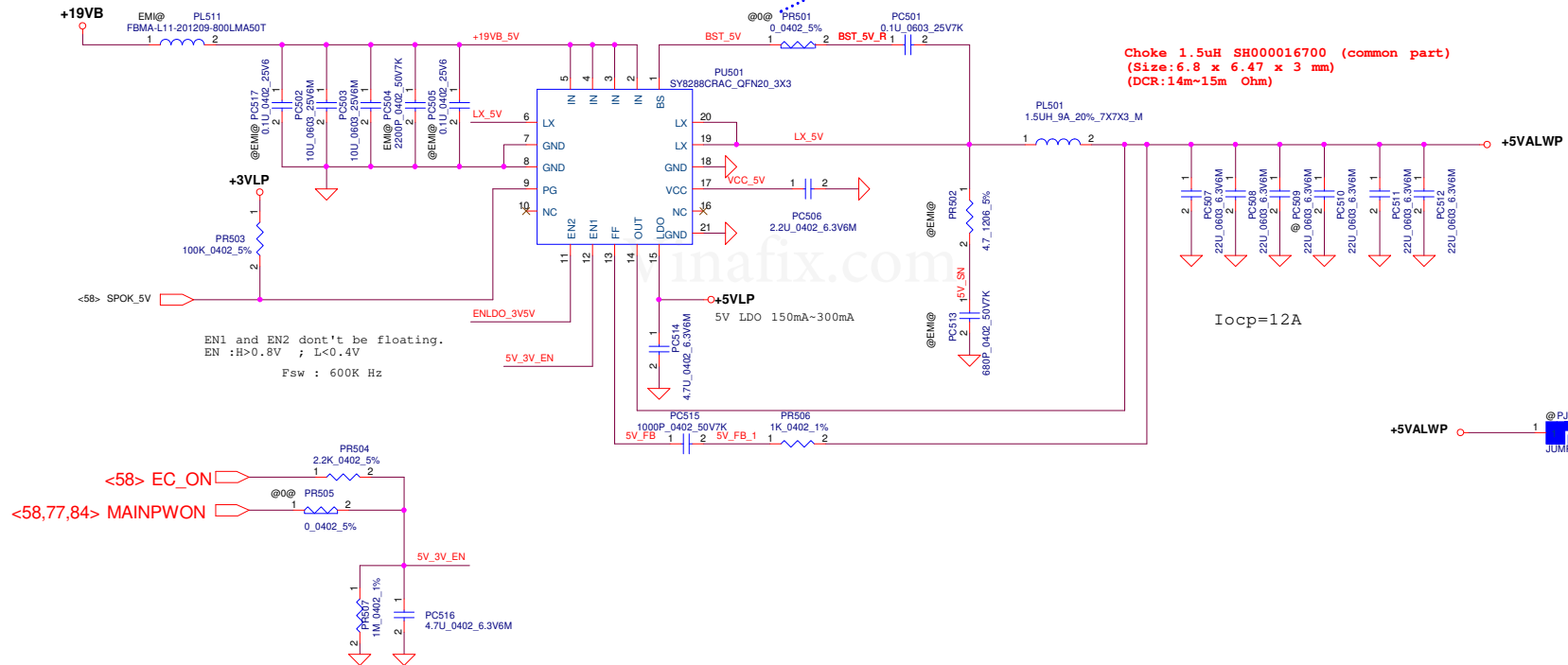


$$ADP_I = 20 * I(\text{adapter}) * 0.01$$
$$I(\text{adapter}) = \text{adapter}(W) * 130\% / 19$$



www-teknisi-indonesia

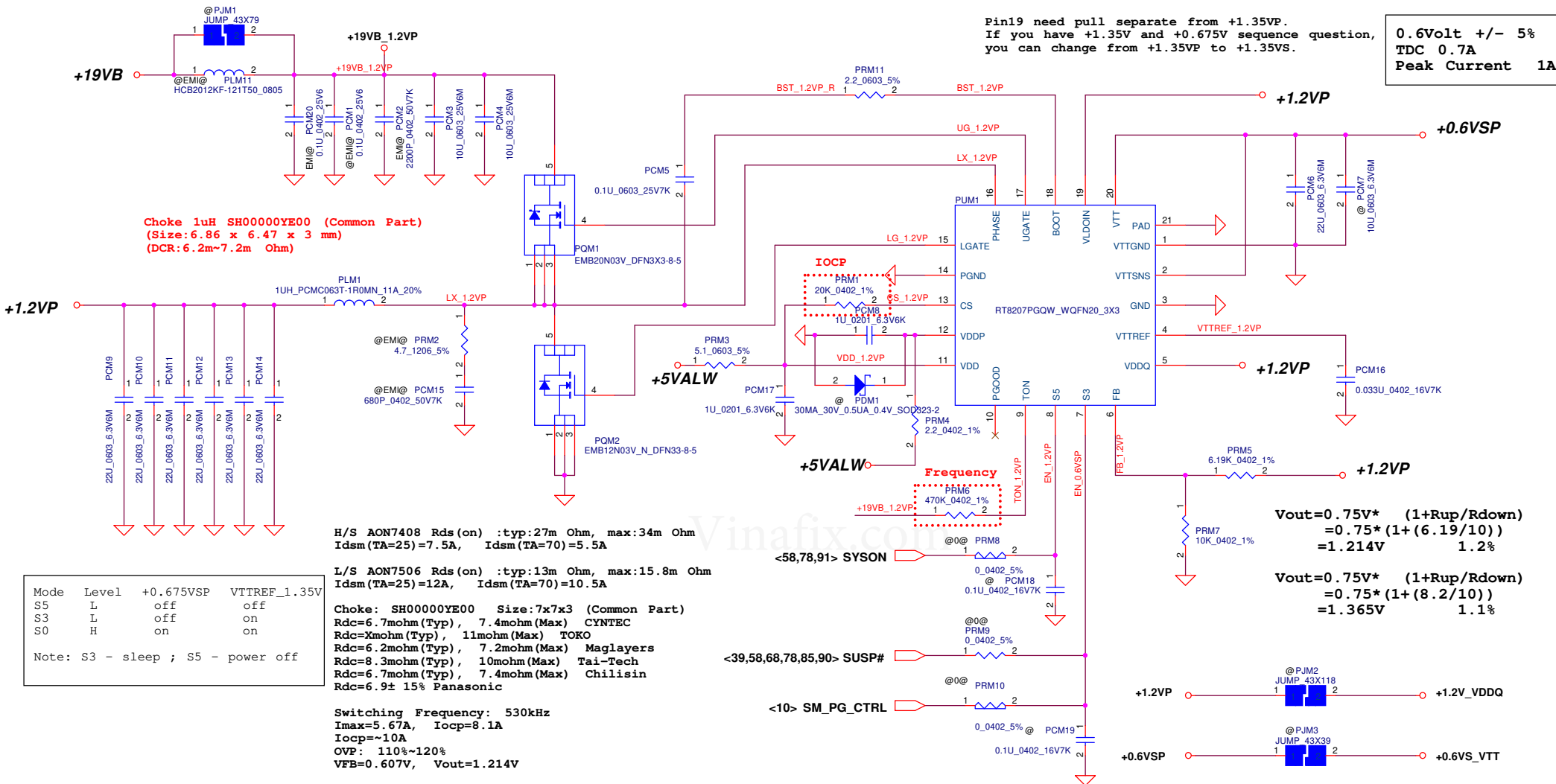
keep short pad,
snubber is for EMI only.



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Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13m Ohm, max:15.8m Ohm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

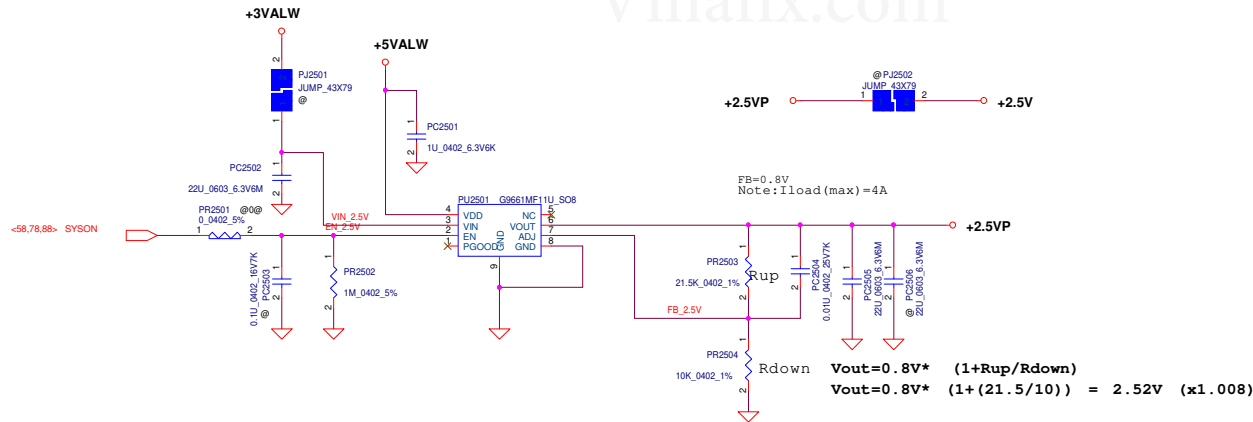
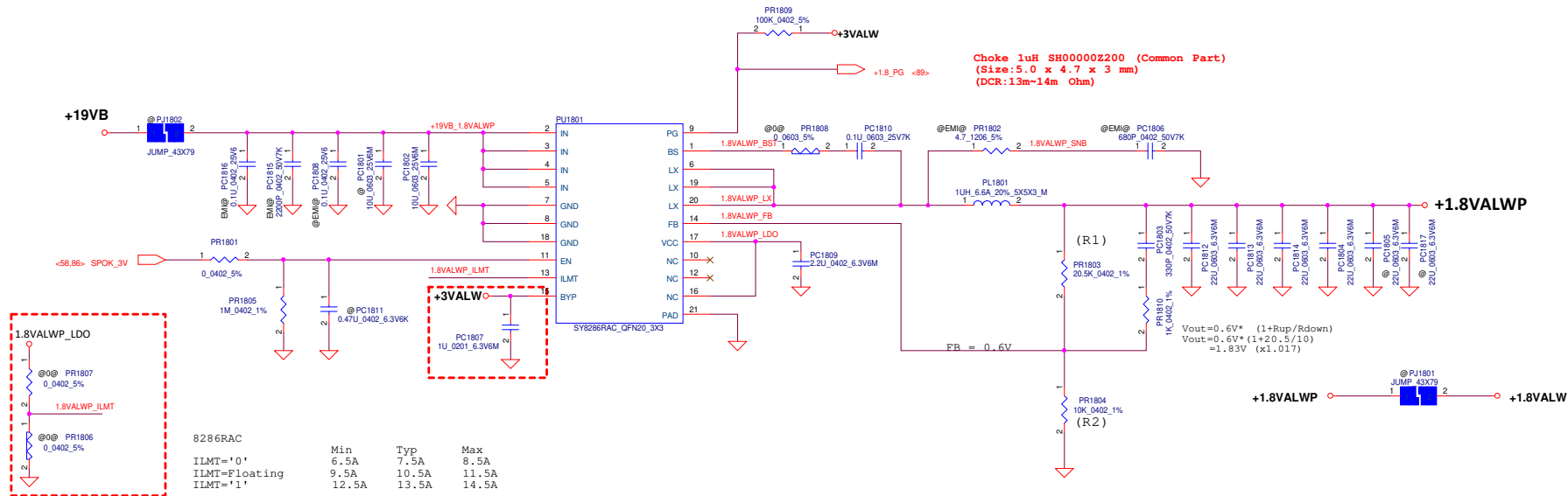
Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilisin
Rdc=6.9± 15% Panasonic

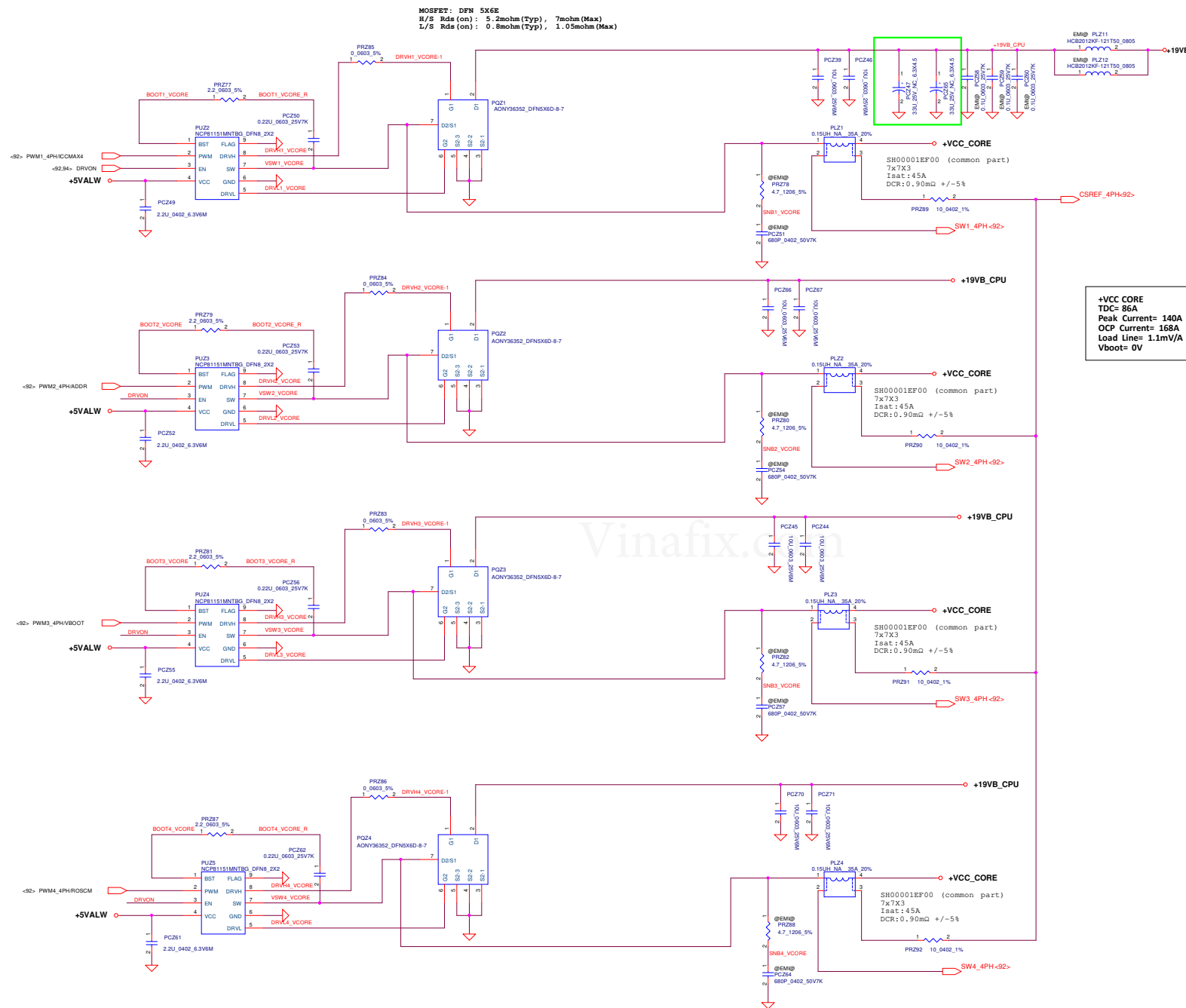
Switching Frequency: 530kHz
Imax=5.67A, Iocp=8.1A
Iocp=~10A
OVP: 110%~120%
VFB=0.607V, Vout=1.214V

$$V_{out}=0.75V \cdot \left(1 + \frac{R_{up}}{R_{down}}\right) = 0.75V \cdot \left(1 + \frac{6.19}{10}\right) = 1.214V \quad 1.2\%$$

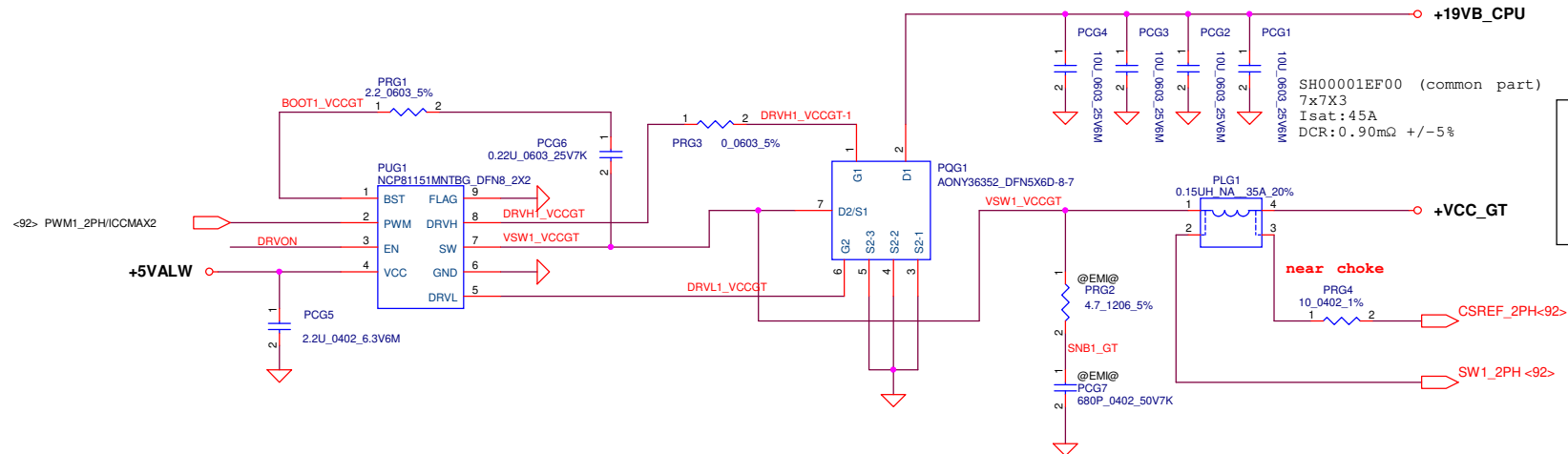
$$V_{out}=0.75V \cdot \left(1 + \frac{R_{up}}{R_{down}}\right) = 0.75V \cdot \left(1 + \frac{8.2}{10}\right) = 1.365V \quad 1.1\%$$

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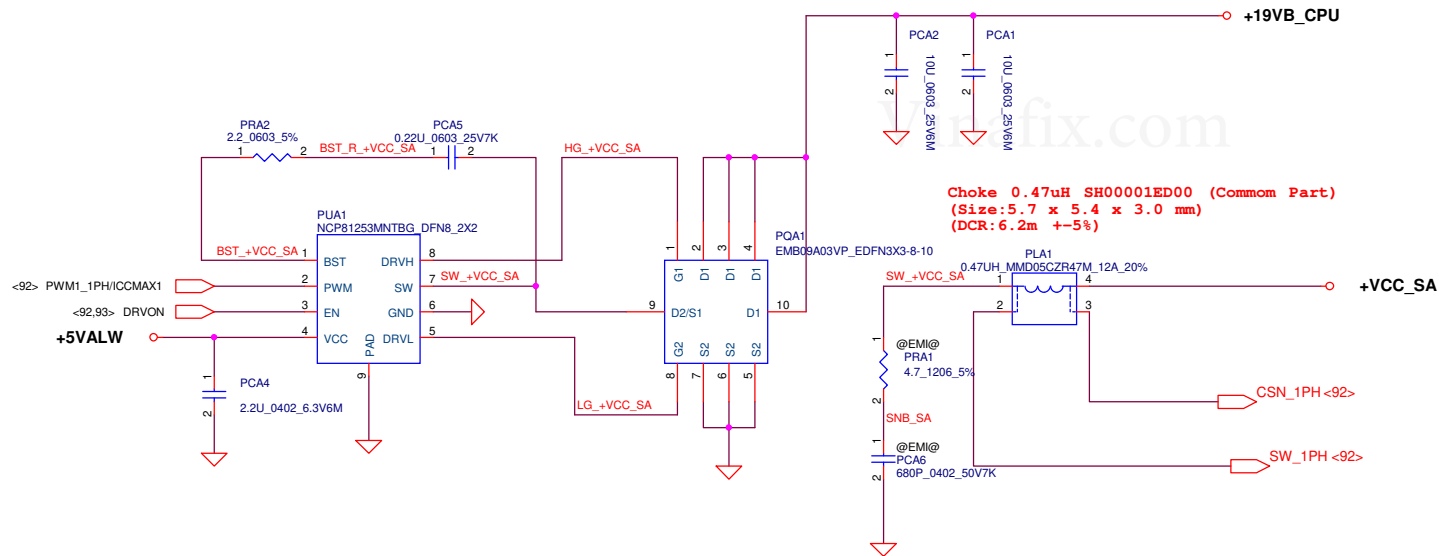




Main Func = VCCGT/+VCCSA

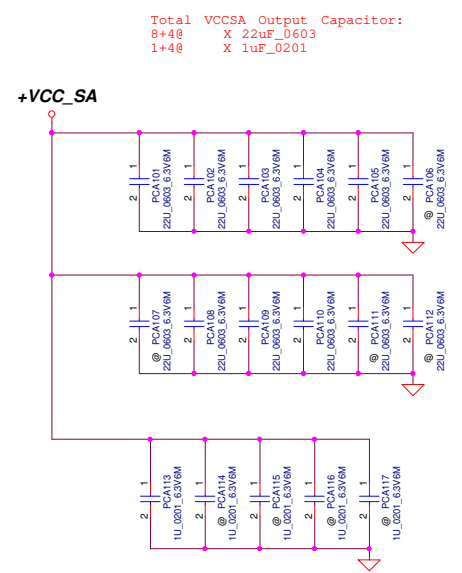
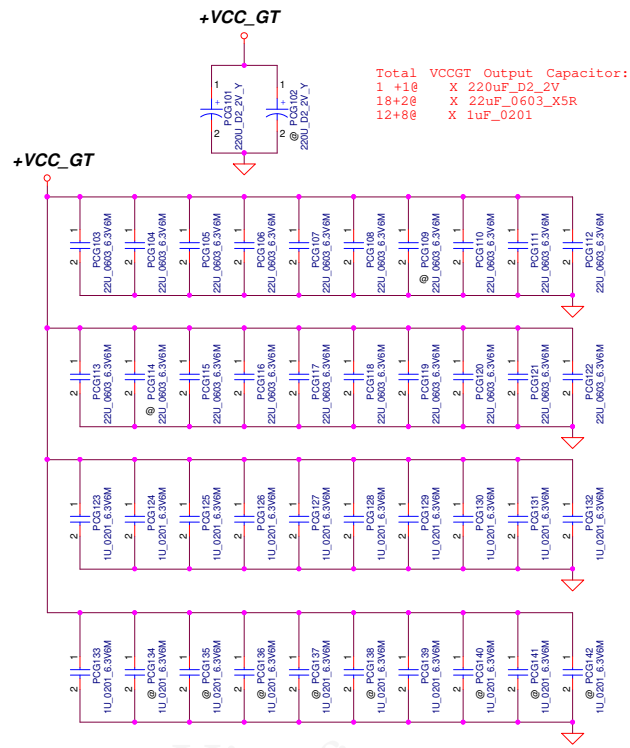
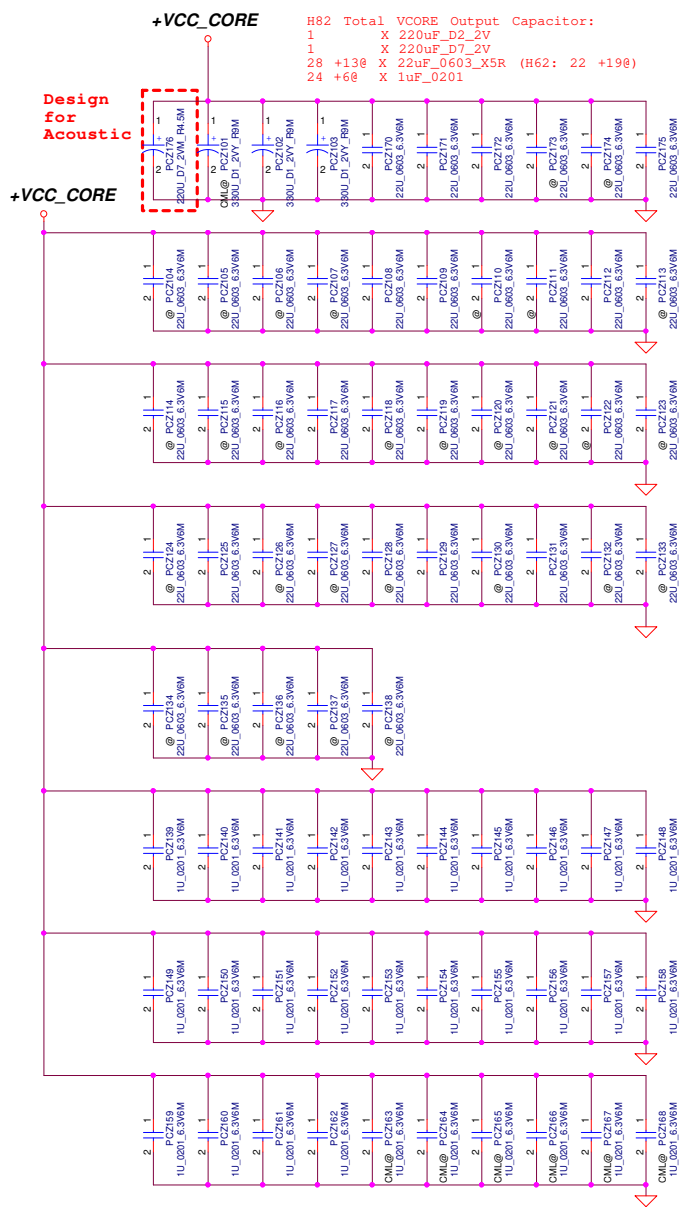


+VCCGT
TDC= 25A
Peak Current= 32A
OCP Current= 39A
Load Line= 2.7mV/A
Vboot= 0V



+VCCSA
TDC= 10A
Peak Current = 11.1A
OCP Current= 13A
Load Line= 10.3mV/A
Vboot= 1.05V

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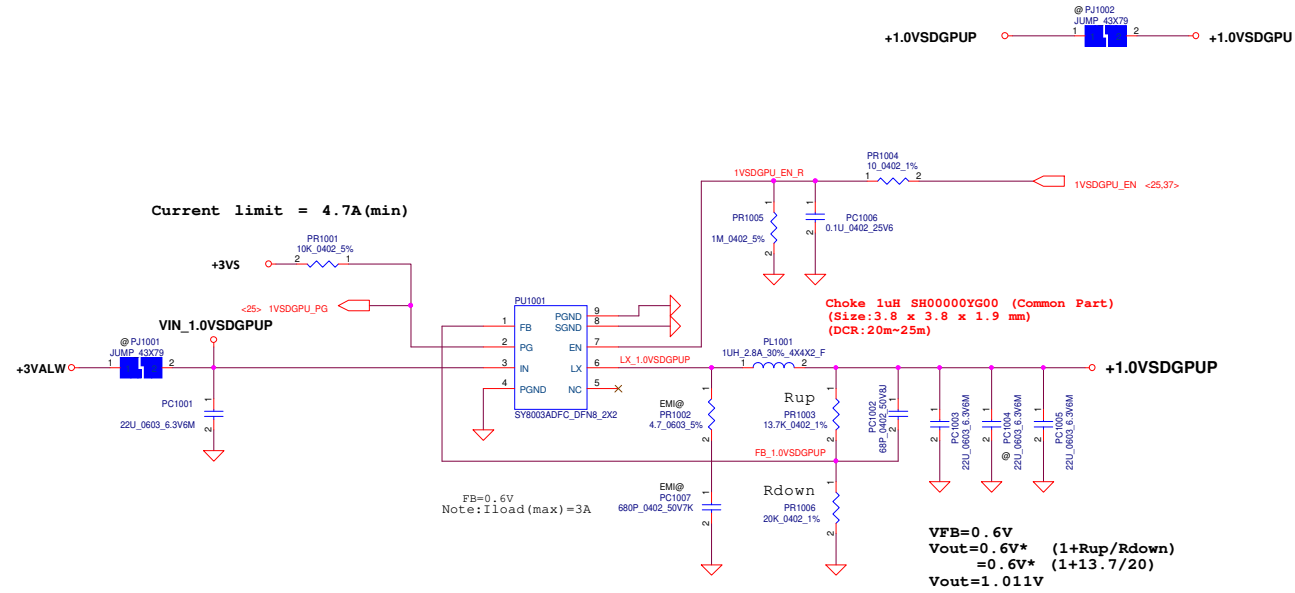


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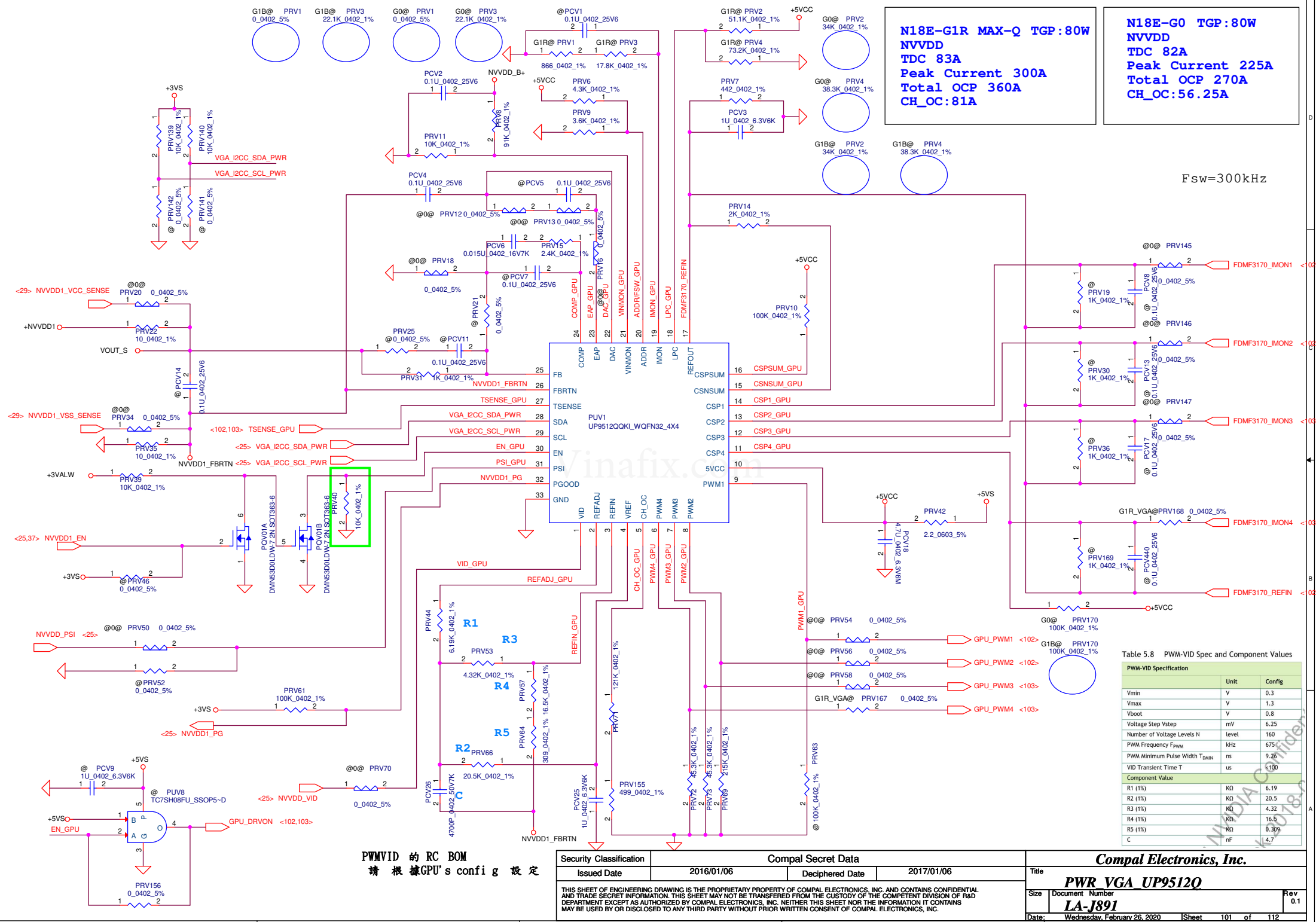
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N18E-G1R MAX-Q TGP:80W NVVDD TDC 83A Peak Current 300A Total OCP 360A CH_OC:81A	N18E-G0 TGP:80W NVVDD TDC 82A Peak Current 225A Total OCP 270A CH_OC:56.25A
---	---

Fsw=300kHz

Table 5.8 PWM-VID Spec and Component Values

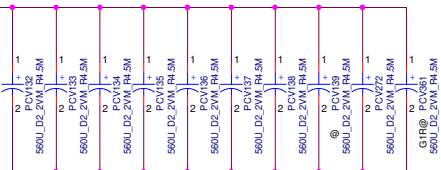
PWM-VID Specification		
	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F _{PWM}	kHz	675
PWM Minimum Pulse Width T _{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

PWMVID 的 RC BOM
請根據GPU's config 設定

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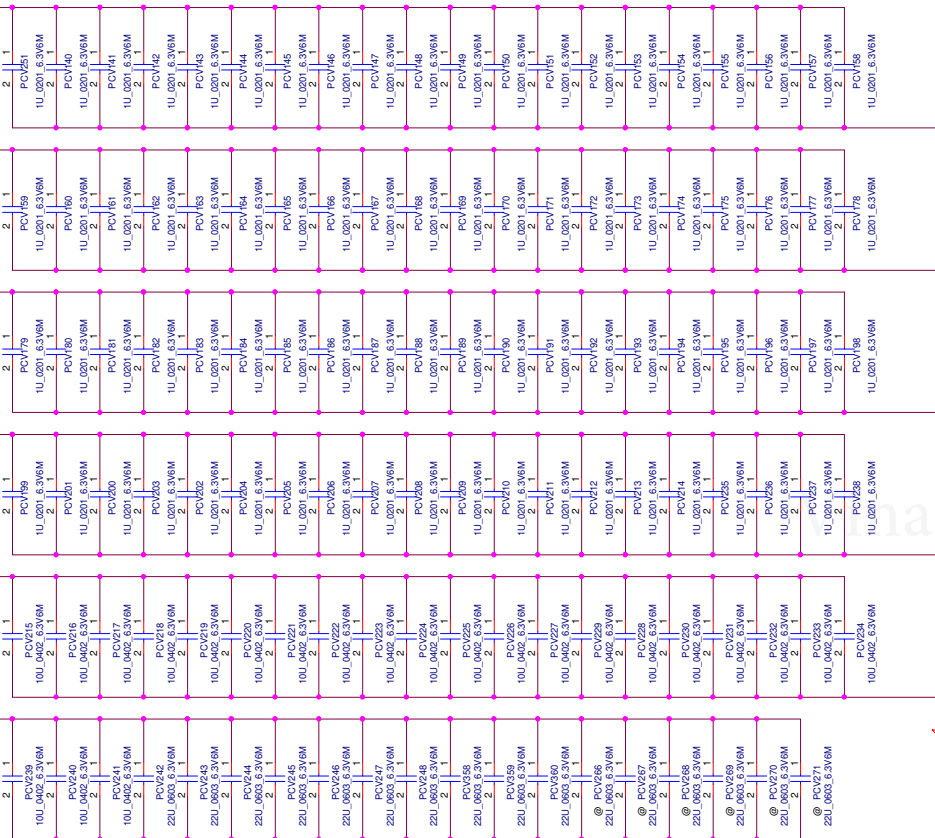
+NVVDD1

Place near GPU



N18E-G1R MAX-Q TGP:80W
+NVVDD
Imax: 83A
Ipeak: 282A
560uF_D2_R4.5 X 10
22uF_0603 X 10 @X6
10uF_0402X 23
1uF_0201 X 113 (93+20)

Place under GPU



+NVVDD1

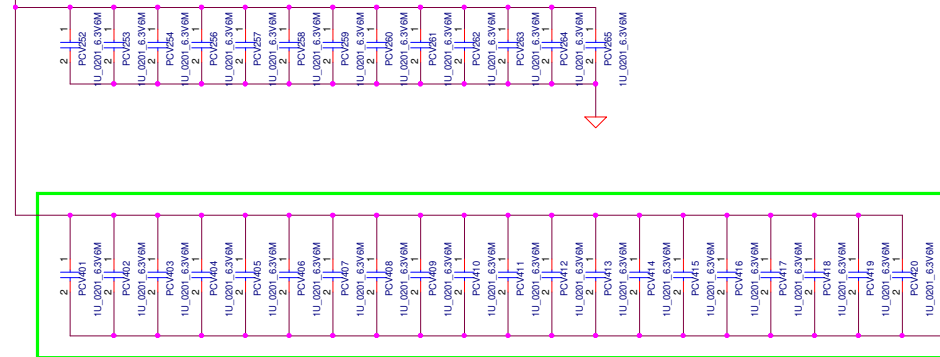


Table 5.10 GB4B-256 Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 x 0.47uF (0201W X65) 23 x 10uF (0603 X65) 4 x 22uF (0805 X65) 3 x 47uF (0805 X65)	2 x 470uF (Poscap)
Alternate solution:				
93 x 1.0uF (0201W X65) 2 23 x 10uF (0603 X65) 4 x 22uF (0805 X65) 3 x 47uF (0805 X65)				

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Reserve VGA thermal sensor	0.1	84	Unpop PH205	11/12	A
02	Design Update	Reserve charger back to back mosfet for verify	0.1	85	Unpop PQB18,19	11/12	A
03	Design Update	Add 330uF for Coffee lake IA core output	0.1	95	Pop PCZ103	11/12	A
04	Design Update	Reserve 6 pcs of 22uF output cap for G1R-MaxQ sku	0.1	104	Unpop PCV266,PCV267,PCV268,PCV269,PCV270,PCV271	11/12	A
05	Design Update	shortage of SA0000AQE00 NCP81215MNTXG	0.1	92	change SA0000AQE00 to SA0000CTW00 NCP81215PMNTXG	11/12	A
06	Byer cost down action	PRB12 down size from 10ohm 1206 to 0805 size	0.2	85	PRB12 change from SD011100A80 to SD002100A80	12/10	B
07	X63ALYBOL01 change from "EGO,G1+CFL" to "EG1B+CML"	VCCORE Set to CML setting	0.2	92 95	1.PRZ47,PRZ50, PRZ52, PRZ54 change from SD014118380(118k) to SD014191380 (191k) 2.PRZ42 change from SD034301280(30.1k) to SD034187280 (18.7k) 3. Add PCZ101 (SGA00009S00) for CML 4. Add PCZ163,PCZ164,PCZ165,PCZ166,PCZ167,PCZ168(SE00000UC00) for CML	12/11	B
08	Design Update	Add PRB47,PRB48,PRB49 for reserving thermal sensing of B to B first MOSFET	0.2	85	Add PRB47,PRB48,PRB49 0 ohm(SD028000080)	12/11	B
09	Design Update	For VCCGT loadline tuning	0.2	92	PRZ49 change from SD034274380(274k) to SD034165380 (165k)	12/16	B
10	Design Update	For VCCSA IMON tuning	0.2	92	PRZ14 change from SD034280280(28k) to SD034294280(29.4k)	12/16	B
11	Design Update	Add 100k pull high 5VCC for disable VGA phase 4	0.2	101	Add PRV170 SD034100380 (100k)	12/09	B
12	Design Update	Setting right VRAM voltage for G1R and G1B GDDR	0.2	99	1.PRW25 change from SD034604280 (60.4k) to SD034374280 (37.4k) 2.PRW23 change from SD034787180 (7.87k) to SD034750180 (7.5k) 3.PRW24 change from SD034261280 (26.1k) and SD034187280(18.7k) to SD034249280(24.9k)	12/12	B
13	Byer cost down action	For lower cost	0.2	85	PCB18 change from SE00000WP00(2.2uF 25V) to SE000006S80 (2.2uF 16V)	12/09	B
14	Design Update	For optmial VCCCORE output cap	0.2	95	PCZ104,PCZ105,PCZ106,PCZ107,PCZ110,PCZ111,PCZ113,PCZ114,PCZ115,PCZ116,PCZ118,PCZ119,PCZ120,PCZ121,PCZ122,PCZ123,PCZ124,PCZ126,PCZ127,PCZ128,PCZ130,PCZ132,PCZ133,PCZ134,PCZ135,PCZ136,PCZ137,PCZ138,PCZ173,PCZ174 change to reserve	12/16	B
15	Byer cost down action	For lower cost	0.2	88	PCM6 change from SE000005T80 (10uF 0603) to SE00000M000 (22uF 0603) PCM7 change to reserve	12/09	B

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02						
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Version change list
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PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5% (SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PR65 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Change the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B
09	Design Update	For ESD request	82	Pop PC205 0.1U_0603_25V7K (SE042104K80) HS 鋁 皮 離 ESD 能量透過 PCB 小板及 H5 cable coupling 造成 干擾	1/15	B
10	Design Update	For EMI request	93, 96	Pop PCW1, PCV48 2200P_0402_50V7K (SE074222K80) for EMI request Pop PCW2, PCV47 0.1U_0402_25V6 (SE000006880) for EMI request	1/15	B
11	Design Update	Design change	90, 87	delete boost circuit and PCZ47	5/7	FH58F EVT
12	Design Update	Design change	90, 87	delete PC1112	5/7	FH58F EVT
13	Design Update	Design change	88, 93	change PCB15 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to 1U 16V K X5R 0402(SE000000U00) change PCB16 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to S CER CAP 2.2U 16V K X5R 0402(SE000013780) Add PLV2, PLV3 second source S COIL .22UH TMC1004H-R22MG-R5505-D 50A(SH00001XH00)	6/25	INV2
14	Design Update	change CH_OC to 75A	95	change PRV71 from S RES 1/16W 133K +-1% 0402(SD034133380) to S RES 1/16W 113K +-1% 0402(SD034113380)	6/25	FH58F PVT

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Phase Rev.

Item	Page	Title	Date	Issue Description	Solution Description
1	52	CNVi	1209	CNVi-Intel review (FH5VF)	Add RM67 / RM68 0-ohm Add PU RM70 / PD RM69 (Reserve)
2	52	UART_BT	1209	UART_BT review	RM66 Change to @ for Vender review
3	17/69	JSSD3	1209	JSSD3 SATA/PCIE detect	SATA6P change to 6P4 & RH303 PU
4	64	EMR	1209	EMR Power source	RH285/RH286/RH292 power source change to +3VALW
5	19	PROJECT ID	1209	PROJECT ID	defined as Project - 60 (ID1:H / ID0:H)
6	38	Panel OD	1209	Panel OD function	RX11 change to unpop & BIOS needs to detect panel to select H or L .
7	16/58	BT_ON	1209	BT_ON change to PCH	RH304 pop (PCH) & RB85 unpop (EC)
8	15/68/69	M.2 SSD	1209	Fixed naming	> SSD1 - GPP_B9/CLKREQ4# (PCIE only) (2018 @SSD2) > SSD2 - GPP_B8/CLKREQ3# (PCIE/SATA) (2018 @SSB1) > SSD3 - GPP_B10/CLKREQ5# (PCIE/SATA) (2019 NEW) > PEDET naming
9	52	CNVi	1209	CNVi-Intel review (FH5VF)	RM70 change power source to +3VS_WLAN
10	58	Board ID	1209	Board ID config	ADD DVT@ & DVTR6B@ for DVT BOM
11	18/23/58/63	DRAM/SYSON/TP	1209	ESD	> Add CH55 33p & EDS@ > Change CD10 to XESD@ > Change CB12/CB13 to 33p & ESD@ > Add CK203 680p & ESD@
12	58	EC	1209	EC_SMB_CK3/DA3	> RB79/RB80 change power source to +5VS
13	81-111	PWR SCH	1209	POWER update	Combined Power SCH (1209A)
14	77	Screw Hole	1210	DDR Shielding	> Add CLIP11
15	81-111	PWR SCH	1210	POWER update	Combined Power SCH (1210A)
16	81-111	PWR SCH	1210A	POWER update	Combined Power SCH (1210B)
17	52	CNVi	1211	CNVi-Intel review (FH51M)	> RM69 change to 71.5k & CNVI@ > RM70 set CNVI@ > RH22 change to 20K > RM36/RM37/RM67/RM68 change to 22 ohm
18	73	IO_B conn.	1211	IO_B conn.	> Change IO_B pin definition
19	69	SSD3	1211	BOM Config	> ADD "SSD3@" for BOM
20	81-111	PWR SCH	1213	POWER update	Combined Power SCH (1213)
1	20/3842/56	PCH/eBP/Type-C/Audio	0113	BOM Config / Short pad	> Change RH100/RS137/RA9 to short pad > Change RX8/RX9/RA14 BOM structure to EMI@
2	81-111	PWR SCH	0113	POWER update	Combined Power SCH (0113)
3	81-112	PWR SCH	0115	POWER update	Combined Power SCH (0115)
4	16	PCH	0115A	ROM co-lay	> Delete JC1 for co-lay
5	81-113	PWR SCH	0116	POWER update	Combined Power SCH (0115B)

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